B-Channel Resynchronizer

Description

ISDN public networks (CENTRAL OFFICES) usually implement channel switching except on leased lines. When higher data rates than 64 kbps are required between two terminals or between a terminal and a server or host machine, and normal ISDN connection is used, it is necessary to group several B channels. The central office does not ensure that the grouped B channels will be affected by a similar group delay (multiple of 125 µs), because the B channels can take different routes across the network.
The 29C98 circuit is specially designed to measure the differential group delay on designated channels, and use the measurements to program a complementary delay in order to obtain correct synchronization between the grouped B-channels.
This feature is required in high speed ISDN connection, such as Router, Multiplexer, Hub etc...
The 29C98 B-CHANNEL RESYNCHRONIZER CIRCUIT is placed between 2 PCM serial links in order to resynchronize different timeslots and create well aligned hyperchannels, such as CCITT H channels.
The circuit can support different types of concatenated channels such as :
- 15 times 2 B channels together
- one time 30 B channels

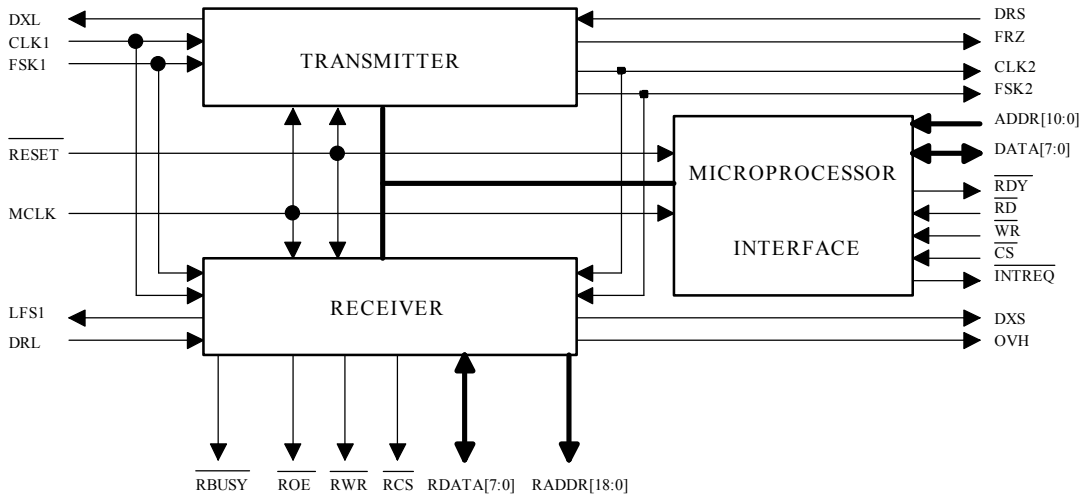
The first example corresponds to the concatenation of B1 and B2 channels on 15 different ISDN Calls. The second corresponds to the concatenation of all possible channels for one Call on an ISDN primary access (CCITT H12 Hyperchannel).
B channel resynchronization may be required when an application uses more than 64 kb/s of bandwidth. Such an application can be multiplexed into several 56 or 64 kb/s channels, and these channels are transmitted individually. The routing of these channels, hence their delays, may not be equal from one channel to the next. After other devices multiplex these 56 or 64 kb/s channels into a single high-speed bit stream, it is the task of the 29C98 to reorder the data into its original form, with equalized delay.
A 29C98 circuit must be present at each end point. As the 29C98 uses an external delay RAM, the user can optimize its configuration for his application. The maximum RAM size will authorize the equalization of 32 channels with a maximum of 2 second delay between the fastest and the slowest channel.

Features

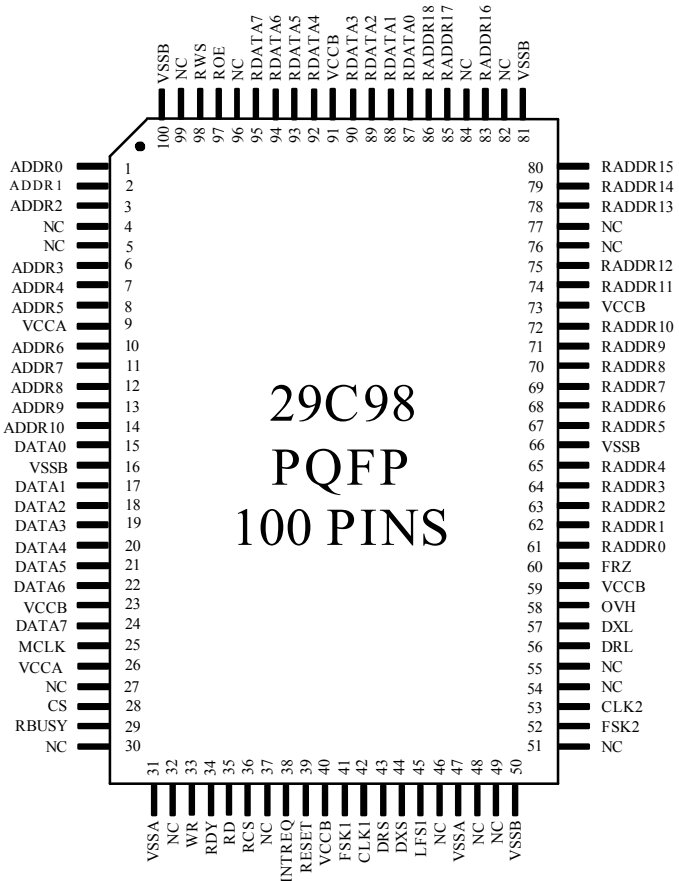
- B-Channel Delay Equalization according to BONDING - ISO/IEC DIS 13871 Standards.
- Supports BONDING - ISO Modes 0, 1, 2 and transparent.
- Single Chip CMOS Monolithic Device simplifies ISDN/DMI Implementation.
- Provides differential Group Delay detection and compensation between CEPT or T1/DS1 PCM time slots, for up to 32 different time slots.
- Provides resynchronization of CCITT I412 Hyperchannels
  - H0 (384 Kb/s)
  - H11 (1536 Kb/s)
  - H12 (2048 Kb/s)

  and user defined Hyperchannels.
- Compatible with MHS 29C94 Multichannel Protocol Controller and 29C96 Framer Formatter.
- Compatible with 2.048 Mb/s CEPT and 1.544 Mb/s T1/DS1 framing format.
- 2.048 Mb/s CEPT or 1.544 Mb/s T1/DS1 PCM interface toward line.
- 2.048 Mb/s CEPT or 1.544 Mb/s T1/DS1 PCM interface toward system (equalized).
- Parallel 8 bit data bus, 12 bit address bus.
- System clock input 16 MHz to 30 MHz.
- Programmable channel by channel loop back mode.
- Operates from a single 5 V Power supply.
- 100 pin PQFP package.
- Can equalize up to 2 seconds of relative delay.
- External RAM for delay equalization with dedicated data (8 lines) and address (19 lines)

Block Diagram



Pin Configuration



NC = NOT CONNECTED

Pin description

Pin	Name	Type	Description
1 to 3	ADDR[0:2]	I	Microprocessor address bus bit 0 to 2
6 to 8	ADDR[3:5]	I	Microprocessor address bus bit 3 to 5
10 to 14	ADDR[6:10]	I	Microprocessor address bus bit 6 to 10
15	DATA[0]	I/O	Microprocessor data bus bit 0
16	VSSB	SUPPLY	Ground
17 to 22	DATA[1:6]	I/O	Microprocessor data bus bit 1 to 6
23	VCCB	SUPPLY	5 V (+/- 10%)
24	DATA[7]	I/O	Microprocessor data bus bit 7
25	MCLK	I	Microprocessor clock, 16 to 30 MHz
26	VCCA	SUPPLY	5 V (+/- 10%)
28	CS	I	Chip Select (active low)
29	RBUSY	O	Delay RAM buses are busy (driven by the 29C98, active low signal)
31	VSSA	SUPPLY	Ground
33	WR	I	Microprocessor write signal (active low)
34	RDY	O	Ready : a low level on this signal indicates that the command signal can be removed (data valid on DATA[7:0] during read operation or data stored in the 29C98 during write operation).
35	RD	I	Microprocessor read signal (active low)
36	RCS	O	Delay RAM chip select (active low)
38	INTREQ	O	Microprocessor interrupt request (active low - open collector)
39	RESET	I	Reset signal (active low)
40	VCCB	SUPPLY	5 V (+/- 10 %)
41	FSK1	I	Frame synchronization clock (8 KHz signal). Indicates the first channel of the PCM frame (on the line side).
42	CLK1	I	Bit clock (1.544 MHz or 2.048 MHz, line side).
43	DRS	I	PCM serial data link input (system side)
44	DXS	O	PCM serial data link output (system side)
45	LFS1	O	PCM line timing error (active 1)
47	VSSA	SUPPLY	Ground
50	VSSB	SUPPLY	Ground
52	FSK2	O	Frame synchronization clock (8 KHz signal). Indicates the first channel of the PCM frame (system side).
53	CLK2	O	Bit clock (1.544 MHz or 2.048 MHz, system side).
56	DRL	I	PCM serial data link input (line side)
57	DXL	O	PCM serial data link output (line side)
58	OVH	O	BONDING Overhead byte reception (active high). This signal is generated one PCM frame in advance in order to indicate to the device connected on DXS pin that it will have to ignore the reception of the current Timeslot number in next PCM frame.
59	VCCB	SUPPLY	5 V (+/- 10%)
60	FRZ	O	Freeze (active high). This signal indicates a BONDING overhead byte transmission. The device connected on DRS pin must skip the current Timeslot.
61 to 65	RADDR[0:4]	O	Delay RAM address bus, bit 0 to 4
66	VSSB	SUPPLY	Ground
67 to 72	RADDR[5:10]	O	Delay RAM address bus, bit 5 to 10

Pin description (continued)

Pin	Name	Type	Description
73	VCCB	SUPPLY	5 V (+/- 10%)
74	RADDR[11]	O	Delay RAM address bus, bit 11
75	RADDR[12]	O	Delay RAM address bus, bit 12
78 to 80	RADDR[13:15]	O	Delay RAM address bus, bit 13 to 15
81	VSSB	SUPPLY	Ground
83	RADDR16	O	Delay RAM address bus, bit 16
85 to 86	RADDR[17:18]	O	Delay RAM address bus, bit 17 to 18
87 to 90	RDATA[0:3]	I/O	Delay RAM data bus, bit 0 to 3
91	VCCB	SUPPLY	5 V (+/- 10 %)
92 to 95	RDATA[4:7]	I/O	Delay RAM data bus, bit 4 to 7
97	ROE	O	Delay RAM output enable signal (active low)
98	RWS	O	Delay RAM read/write signal (write active low)
100	VSSB	SUPPLY	Ground
	NC	-	Not Connected

Functional description

The circuit includes three main blocks (see block diagram above) :

- Receiver
- Transmitter
- Microprocessor interface

Note : in the following we will refer to Line side (interface with a framer) or System side (interface with the protocol controller). In the same way, the non equalized time slots will be named TSL (Line side) and the equalized time slots will be named TSS (System side). Some description are based on a 32 time slot PCM bus. Take care that with a 24 time slot PCM bus, some hardware resources (registers...) are no more available.

Receiver

On one side, the receiver accepts a primary rate serial data link (PCM at 2.048 or 1.544 Mb/s not delay equalized) from the Line through a framer (like 29C96). On the other side, it drives the same type of data (with timeslots reordered and equalized) towards the system, for example a multi channel protocol controller (like 29C94).
The main functional blocks are :

- serial to parallel converter
- alignment and synchronization controller
- Timeslot Context Memory
- Delay RAM controller
- Parallel to serial converter

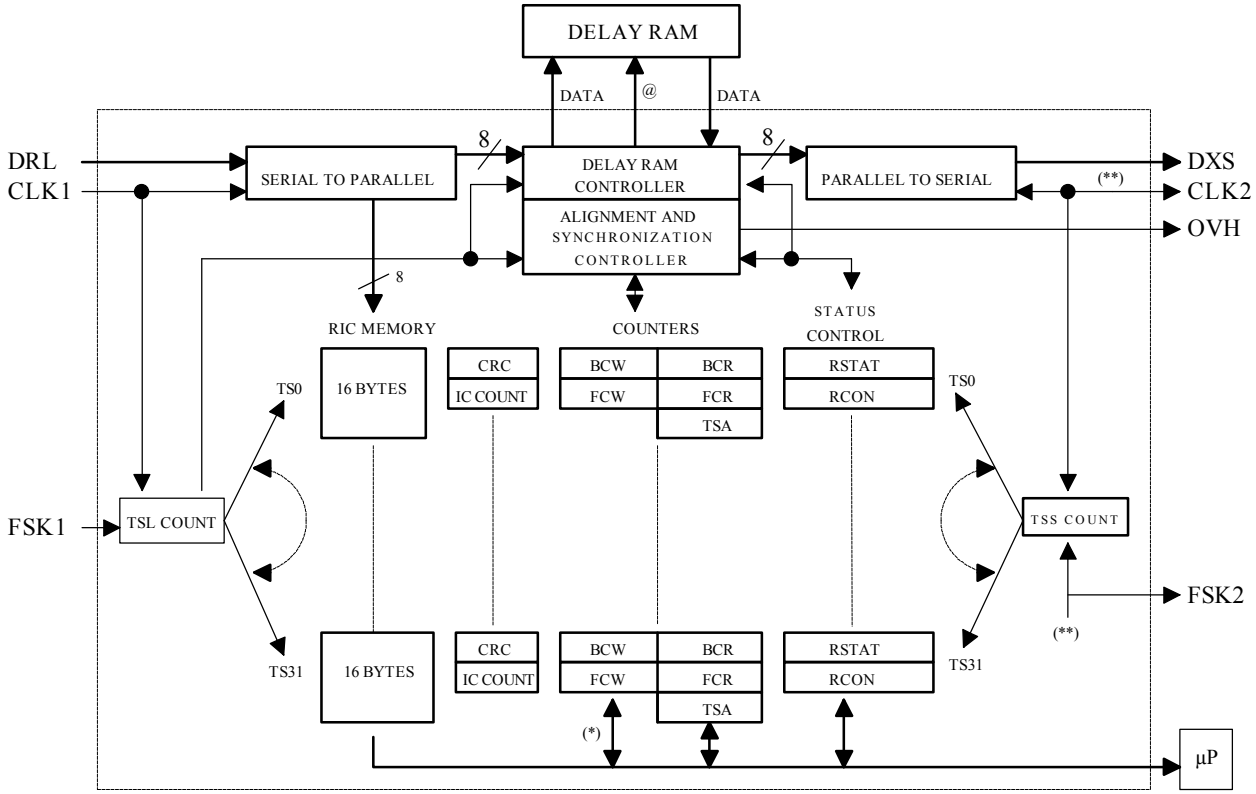
Serial to parallel Converter

Latching of data at pin DRL is done on the falling edges of the clock CLK1. Alignment on Channel 0 of the PCM line is achieved using the frame clock FSK1. Depending on the programming, an optional channel by channel CRC4 calculation is performed (mode 2). If an error is detected, an interrupt is generated.

Alignment and synchronization controller

Each time a new timeslot is received at pin DRL, the controller selects the corresponding Context Memory block.

Figure 1. 29C98, Receiver diagram



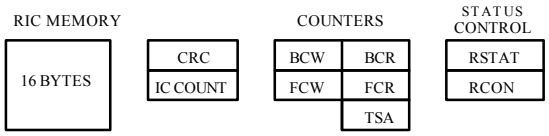
(*) required with external equalization (XSY = 1 in RCON)
(**) internally generated from CLK1 / FSK1

This block is updated following the current step in the BONDING process and the mode (0, 1 or 2).

Timeslot Context Memory

This block includes :

- Control and Status registers
- an IC memory block
- counters and time slot allocation for DMA address calculation
- IC word counter and intermediate CRC4 word



- Receive Control:

Register RCON is used to indicate to the Alignment and synchronization controller the action to be performed according to the BONDING state machine.

- Receive Status :

Register RSTAT informs the µP about the current state of the incoming channel (bit 0 to 2) . An interrupt signal is generated each time a change occurs in RSTAT (except for codes ICFF and ICSF).

- Bit WIC is set to 1 each time a new (valid) data is written in the RIC memory.
- Bits CRC, FC, IC and FAW are set to 1 to mention error conditions (resp. bad CRC4, bad frame count sequencing, Master Channel information or Bonding Frame alignment lost). After a read operation, bit 3 to 7 are cleared to 0.

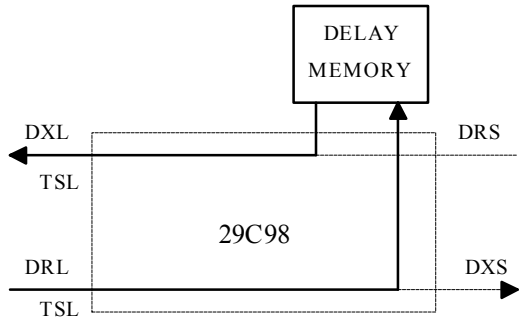
- Time Slot Allocation:

Register TSA is divided into 2 parts :

- a field of 3 command bits :
  - HiZ : when set to 1, the system time slot (TSS) is not driven (High impedance).
  - SSCNT : start / stop counters synchronously (with FSK1). This bit is a toggle bit. When it is used with TRIGG (GLOBAL register), it enables or disables counters FCR, BCR of all the timeslots in the same group.
  - LOOP : the incoming time slot TSL is looped back in the outgoing time slot TSL. The Remote Loopback feature is only available for mode 2 with the 29C98. All the time slots of the call to loop back shall have LOOP=1. The user's data are looped back delay equalized.

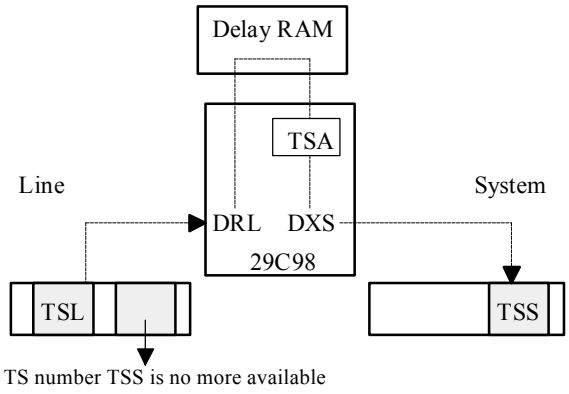
NOTE : the channels are looped back on a TS by TS (physical) basis. The time slot reordering table must be enabled in transmission (ENSTAT=1).

Figure 2. Loop back



- a time slot number to perform time slot reordering :
  - TSL (contained in register TSA) is the time slot number (0 to 31) on Line side associated to the current time slot on the System side (TSS).

Figure 3. Time slot allocation



Note : after reordering, time slot number TSS on line side is no more available.

- RIC memory :

Blocks used to store the 15 bytes of the incoming Information Channel, plus one byte that contains information about the Remote End (received in the Bonding Frame in mode 1 or 2) :

- bit A (=1 when the Remote End is aligned),
- bit E (=1 when a CRC4 error has been detected by the Remote End).
- Bit NCRC (indication that the CRC4 procedure is not supported by the Remote End) is set to 1 when the 29C98 detects three consecutive '1111' sequence in the CRC4 field, with a bit E

set to 0 (no CRC4 error). The user shall then program a code with the bit 3 = 0 in RCON (to disable the CRC4, i.e. codes 0 to 7 depending on the current BONDING step). If bit 3 is left set to 1 with NCRC=1, the incoming CRC4 will be checked continuously and will generate a CRC error .

An interrupt is generated each time a change is recorded in the RIC Memory (bit WIC). To avoid spurious interrupt generation, a field is updated (considered as valid) only when the new value is stable during two consecutive IC frames. The RIC memory is used in mode 0, 1, 2 during the negotiation process (Master Channel), in mode 1, 2 to equalize the delays and in mode 2 during the data transfer phase (monitoring).

- Counters (mode 1, 2) :
  - During the data transfer phase, FCW (0 to 63) and BCW (0 to 255) are used as pointers by the "Delay Ram Controller" to store the data from one incoming TSL, into the external Delay Ram.
  - Byte Count BCR and Frame Count FCR can be used to calculate the relative delay between the channels of the same call (all the channels must be at state ICSVAL in RSTAT, see "Operating sequences"). They are also used as pointers by the "Delay Ram Controller" to read the data back from the external Delay Ram (delay equalized). They are initialized by the user just before switching to data transfer phase.

Delay RAM Controller

The "Delay Ram Controller" is used with BONDING mode 1 and 2 to perform the delay equalization when in the "data transfer" phase (see figure 4). The controller takes the data bytes coming from the Serial to parallel converter and write them into a maximum 512 KByte Delay RAM device at a position that depends on the relative delay between the time slots (write operation @ FCW*8192 + BCW*32 + TSL). Under the control of the system interface, the "Delay Ram Controller" reads the data back from the Delay memory and write them in a parallel to serial converter (read operation @ FCR*8192 + BCR*32 + (TSA)).
Figure 5, 6 hereafter (Delay RAM controller / write and read operations) show the read and write operations for a single physical channel received on DRL :

- Write operation : the address is calculated using the counters BCW, FCW from the context memory block of the time slot.

Figure 4. Delai equlization - Basic

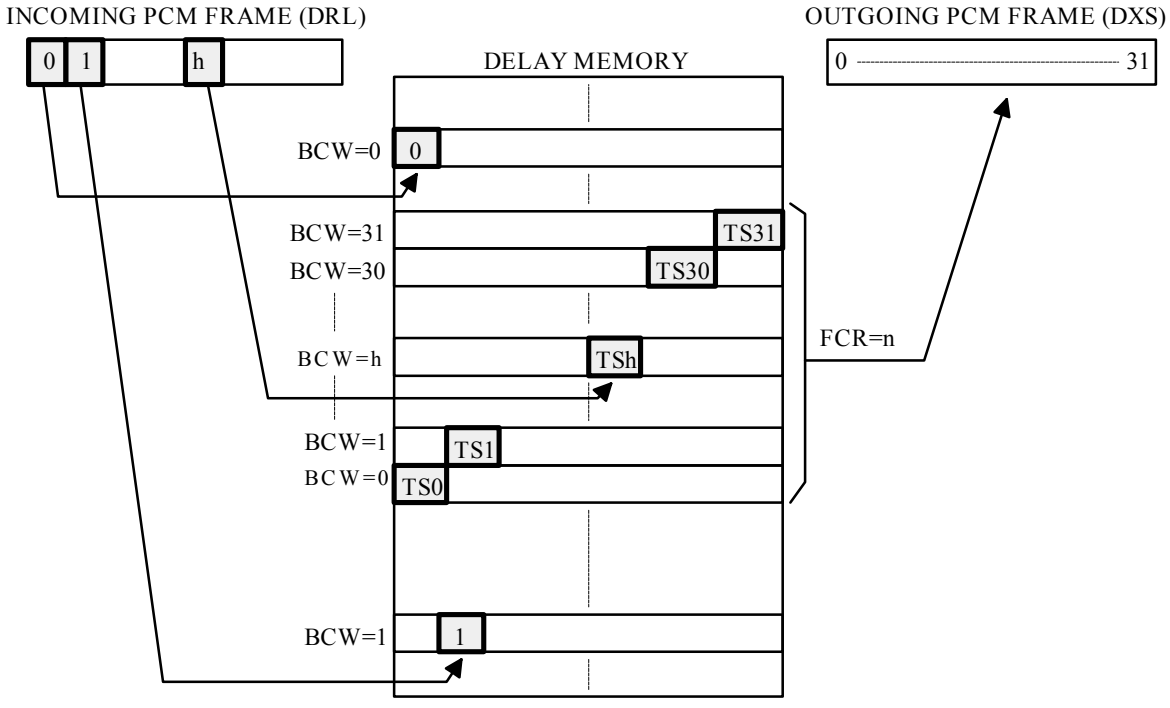


Figure 5. Delay RAM controller - write operation

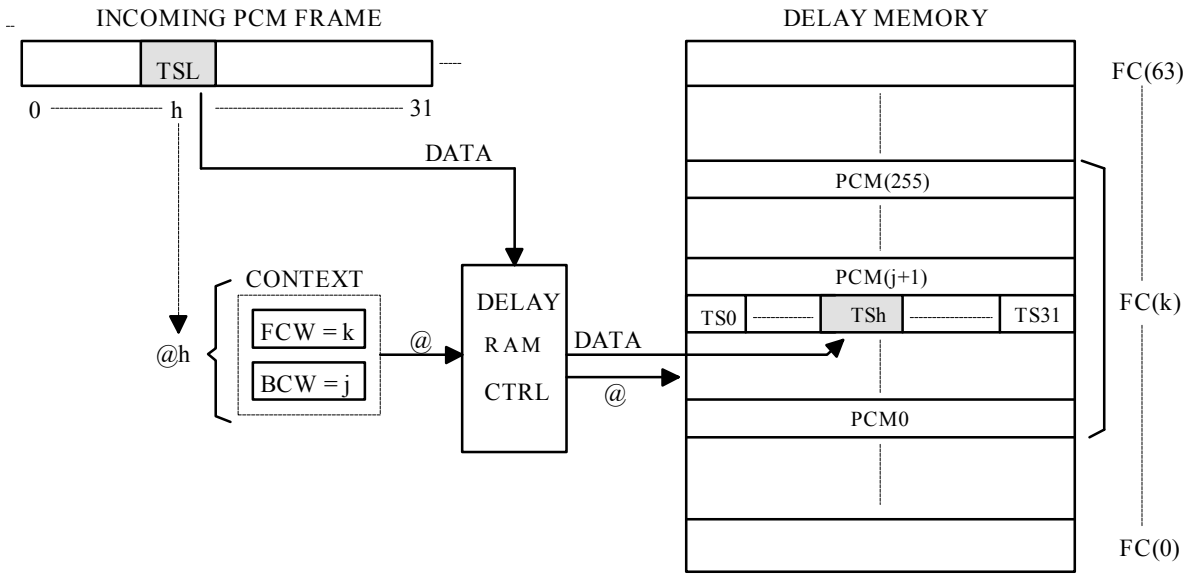
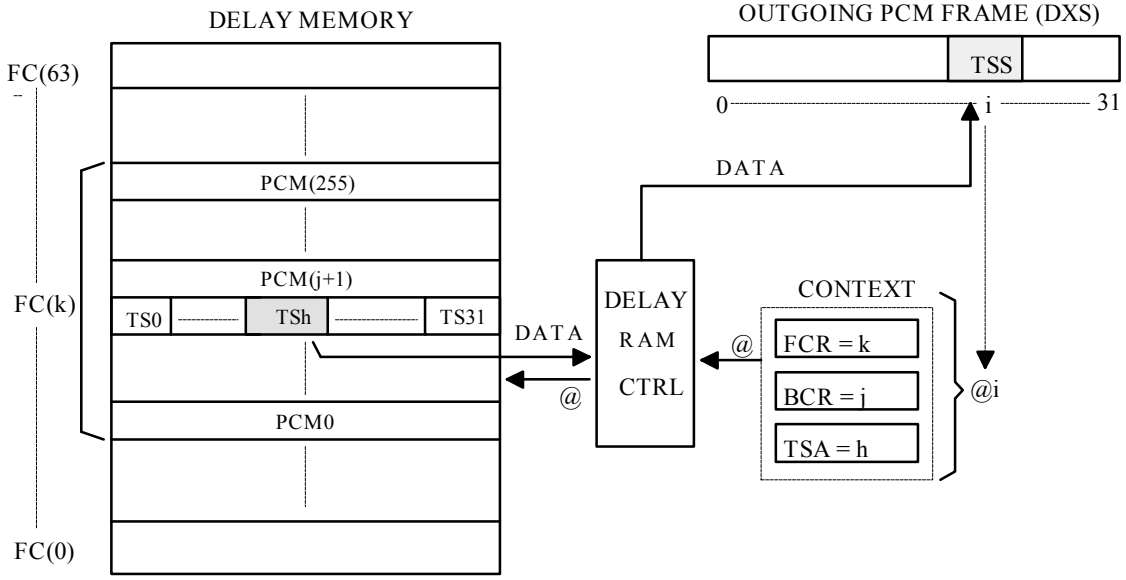


Figure 6. Delay RAM controller - read operation



- The current incoming time slot is TSL = h.
- The associated context block gives FCW = k, BCW = j.

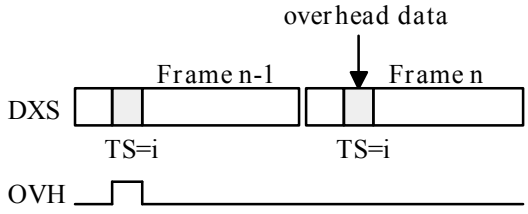
- the data is written at address :
  (k * 8192) + (j * 32) + h

- Read operation : the address is calculated using the counters BCR, FCR from the context memory block of the time slot.
  - The current outgoing time slot is TSS = i.
  - The associated context block gives FCR = k, BCR = j, and TSA = h (time slot h on line side corresponds with time slot i on system side).
  - the data is read at address :
    (k * 8192) + (j * 32) + h

Parallel to serial converter

This block receives 8 bits of data from the Delay memory and serializes them at output DXS on CLK2 rising edge. When in mode 2, the transmission of a BONDING overhead octet on DXS (which shall be ignored) is indicated to the system side one frame earlier by the signal OVH.

Figure 7. Overhead data



n = 63, 127, 191, 255

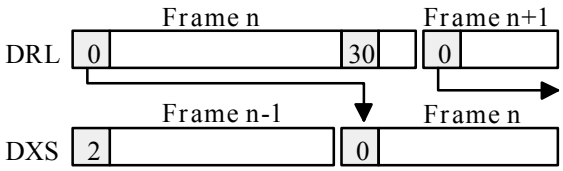
Transparent mode

The transparent mode is possible by programming code TRSP in both registers RCON and TCON.

Delay RAM : in transparent mode, data received in time slots TSL are written in the Delay RAM at address TSL (BCW = FCW = 0, i.e. only the first 32 bytes of the delay RAM are used).
Time slot allocation is possible in transparent mode : in that case, the data to be sent in Time slot TSS on the system side is read in the Delay Ram at address TSL instead of address TSS (TSL has to be written in TSA register).

Latency : there is a maximum delay between write and read operations of 32 x TS and a minimum of 3 TS (depending on the Time slot Allocation register TSA, 30xTS if TSA=TSS=TSL).

Figure 8. Latency in Transparent mode



External delay equalization

When an external delay equalization mode is chosen (XSY=1 in both register RCON and TCON) the counters BCW and FCW must be initialized. The delays between channels have to be determined (outside the 29C98 with a special framing or other means). When the delays are known, the µP has to fill the FCW / BCW counters (@ 460h to 49Fh). Then, counters FCR / BCR shall be initialized according to the user protocol (typically at the same value which can be the FCW / BCW chosen for the slowest time slot).

Example of time slot allocation

A Call uses TSL0, TSL4, TSL6, TSL8 and TSL9.

- RECEIVER SIDE : we receive the TS with the associated CID as follows :

  - TSL0 with CID=1
  - TSL4 with CID=2
  - TSL6 with CID=5
  - TSL8 with CID=3
  - TSL9 with CID=4

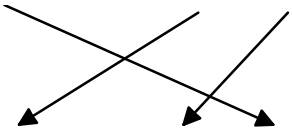
  In order to be able to interface with a 29C94, we must reorder the TS (following increasing order of the CID) :

  - TSL0 sent to 29C94 in TSS0, write 20h @ 4A0h
  - TSL4 sent to 29C94 in TSS4, write 24h @ 4A4h
  - TSL6 sent to 29C94 in TSS9, write 29h @ 4A6h
  - TSL8 sent to 29C94 in TSS6, write 26h @ 4A8h

Figure 9. Time slot allocation example

TSL number :	TSL0				TSL4		TSL6		TSL8	TSL9		
Data :	T				E		C		M	I		
CID :	CID=1				CID=2		CID=5		CID=3	CID=4		

Incoming Frame (DRL)



Outgoing Frame (DXS)

TSS number :	TSS0				TSS4		TSS6		TSS8	TSS9		
Data :	T				E		M		I	C		
CID :	CID=1				CID=2		CID=3		CID=4	CID=5		

- TSL9 sent to 29C94 in TSS8, write 28h @ 4A9h

The diagrams below show the incoming PCM frame (at pin DRL, framer side) and the outgoing PCM frame (at pin DXS, protocol controller side). The data are given as example to understand the TS reordering (the word "TEMIC" is sent, we suppose there is no relative delay between channels).

- TRANSMITTER SIDE : To respect a time slot to time slot correspondence between the receive and the transmit directions (Line side), we must enable the time slot reordering for data coming from the 29C94 (transmit path) by writing bit ENTSAT to 1 in GLOBAL register.

Example of relative delay computation and equalization.

The total duration of a Bonding Multiframe is 2.O48 seconds. With the 29C98, it is possible to compensate 2.048 seconds of relative delay (with an external 512Kx8 memory). But it is possible to measure the relative delays only if the fastest and the slowest channels are separated from less than half this value (1.024 seconds).
The way we can calculate these relative delays is explained hereafter through basic examples (a call that uses TSL2, TSL7, TSL8). Two situations are possible depending on when the internal counters (FCW, BCW) are read.

1) The counters all refer to one single multiframe.

To obtain FCW / BCW stable values, all the timeslots must be at state ICSVAL in RSTAT (IC synchronization with Bonding Multiframe structure) and the procedure explained in chapter "Operating sequences" must be followed. On the figure hereafter, the fastest time slot is TSL7 and the slowest is TSL8. The maximum relative delay between TSL7 and TSL8 is (in frames) :

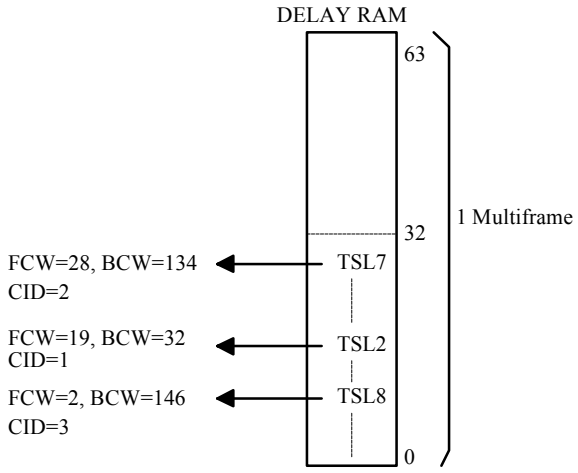
Δ = (28*256 + 134) - (2*256 + 146) = 6644 or 830.5ms.

To equalize the delays, we could write the FCR / BCR using the slowest time slot (here TSL8). The generic formula (for TS number i) :

$$FCR_i = MSB[FCW_8 * 256 + (BCW_8 - CID_i)]$$
$$BCR_i = LSB[FCW_8 * 256 + (BCW_8 - CID_i)]$$

- for TSL2 : FCR=2, BCR=145
- for TSL7 : FCR=2, BCR=144
- for TSL8 : FCR=2, BCR=143

Figure 10. Relative delay computation : FCW/BCW of the same multiframe.



2) The counters do not refer to the same multiframe (fastest time slots are receiving multiframe "n" while slowest time slots are still receiving multiframe "n-1".

The time slots remains TSL2, TSL7, TSL8. On the figure below, the fastest time slot is TSL2 (multiframe n) and the slowest is TSL7 (multiframe n-1). The maximum relative delay between TSL7 and TSL2 is (in frames) :

$\Delta = ((64 - 58)*256 - 134) + (19*256 + 32) = 6298$ or 787.25ms.

or :

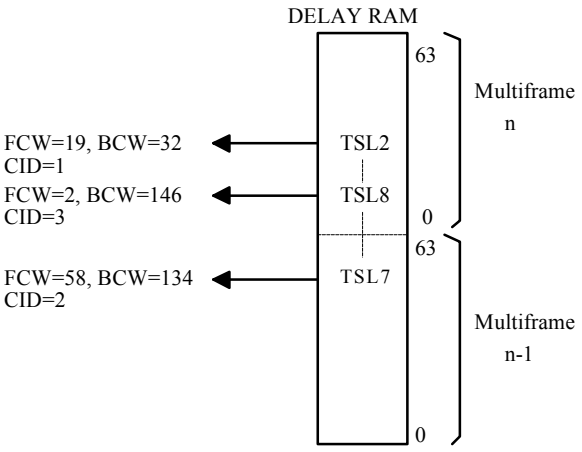
$\Delta = ((64+19)*256 + 32) - (58*256 + 134) = 6298$

To equalize the delays, we could write the FCR / BCR using the slowest time slot (here TSL7). The generic formula (for TS number i) :

$$FCR_i = MSB[FCW_7*256+(BCW_7 - CID_i)]$$
$$BCR_i = LSB[FCW_7*256+(BCW_7 - CID_i)]$$

- for TSL2 : FCR=58, BCR=133
- for TSL7 : FCR=58, BCR=132
- for TSL8 : FCR=58, BCR=131

Figure 11. Relative delay computaion : FCW/BCW do not belong to the same multiframe.



Transmitter

The transmitter accepts a primary rate serial data link (PCM at 2.048 or 1.544 Mb/s) from the system side (29C94 multi channel HDLC protocol controller), it inserts BONDING overhead data in mode 2 and transmits the new data stream towards the line side (29C96 framer).

NOTE : when operating in T1/DS1 mode, the 193rd bit is transmitted unmodified (if EFBIT=0 in GLOBAL register, the bit F is not driven).

The main blocks of the transmitter are :

- serial to parallel converter
- frame buffer
- selector
- TS context memory
- Parallel to serial converter

Serial to parallel Converter

Latching of data at pin DRS is done on the falling edges of the CLK2 clock. Alignment on Channel 0 of the PCM line is achieved using the frame clock FSK2.

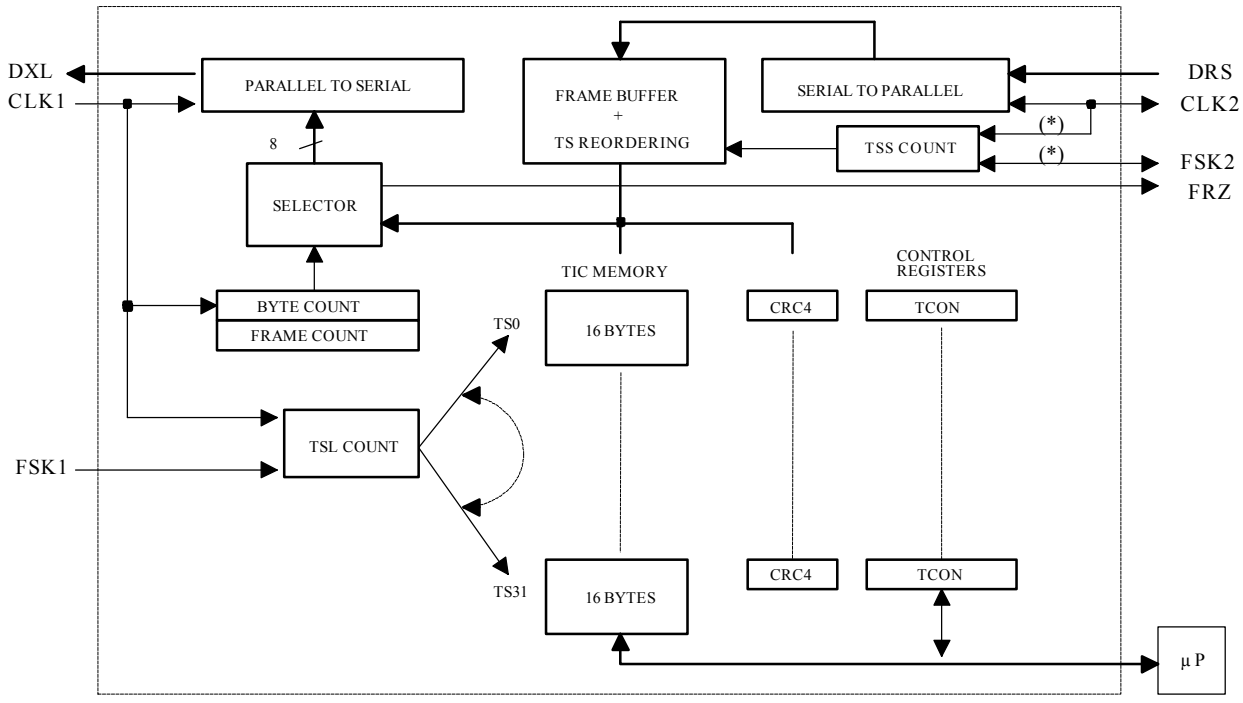
Frame buffer

This buffer is used to store the data received at pin DRS to allow a possible time slot reordering. This time slot allocation is enabled by setting to 1 bit ENTSAT in GLOBAL register. Then, TSA registers of the receiver section are used (the allocation is symmetrical as the one performed by the receiver). If ENTSAT=0, one time slot on the system side corresponds to the same physical time slot on the line side.

Selector

The Selector builds the outgoing stream with the data coming from the frame buffer (and from the TIC memory depending on the mode and on the current step of the BONDING protocol). The Selector uses TSL, FC and BC counters synchronized to the incoming frame pulse (FSK1). The Timeslot counter (0 to 31) TSL selects one amongst the 32 Timeslot Context Memory blocks. The Frame counter will be sent in the BONDING multiframe as FC word (at byte count = 192). The Byte count adjusted with the CID number (to provide the one byte shift of BONDING Multiframe between two consecutive CID of the same call) indicates if the data to send in the current TSL is a user data (read in the frame buffer) or a BONDING overhead byte (read in the TIC).

Figure 12. 29C98, Transmitter diagram



(*) internally generated from CLK1 / FSK1

Timeslot Context memory :

- IC memory block (TIC),
- Control register.
- CRC4 Memory for intermediate values,

- TIC Memory :

Contains the BONDING overhead bytes which are updated by the µP. The format is the same as the RIC memory : The first byte is used to store bits A and E that are part of the CRC4 word of the BONDING Multiframe. The 15 other bytes are IC bytes (the ALIGN word is not stored because automatically generated by the 29C98).

- Transmitter Control register :

TCON is used to tell the Selector what is the next action to perform according to the BONDING State Machine.

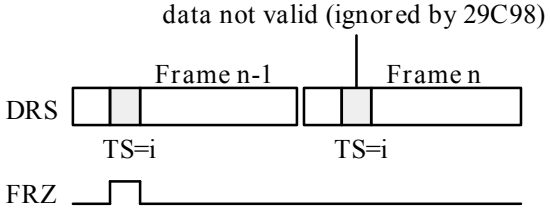
- CRC4 Memory :

It is valid only with communications that use BONDING techniques in mode 2 (with continuous monitoring of transmission quality). The Selector is in charge of the insertion of the CRC4 word in the data stream (when Byte count reaches 255).

Parallel to serial converter

It receives an 8 bit data given by the Selector and serializes them at output DXL on CLK1 rising edge.

Figure 13. Overhead data insertion



n = 63, 127, 191, 255

Because in mode 2, the BONDING overhead octets reduce the bandwidth available for user's data (1/64th of the bandwidth), it is necessary to drive a special FRZ (freeze) signal 125 µs (one frame) earlier to ask the associated protocol controller to cancel the next transmission for this TS on pin DRS (the data shall be sent later, on next PCM frame).

CIDs choice (see figure 14)

In mode 1 and 2, the transmitter has to sequence the channels of a call with the CID. This allow the Remote End to sequence the received channels in proper order.

The user shall assign CID=1 to the initial (Master) channel and shall assign CID in sequential ascending order corresponding to the relative order of the remaining channels. For example, if the word "TEMIC" shall be sent using 3 different time slots, we should always have :

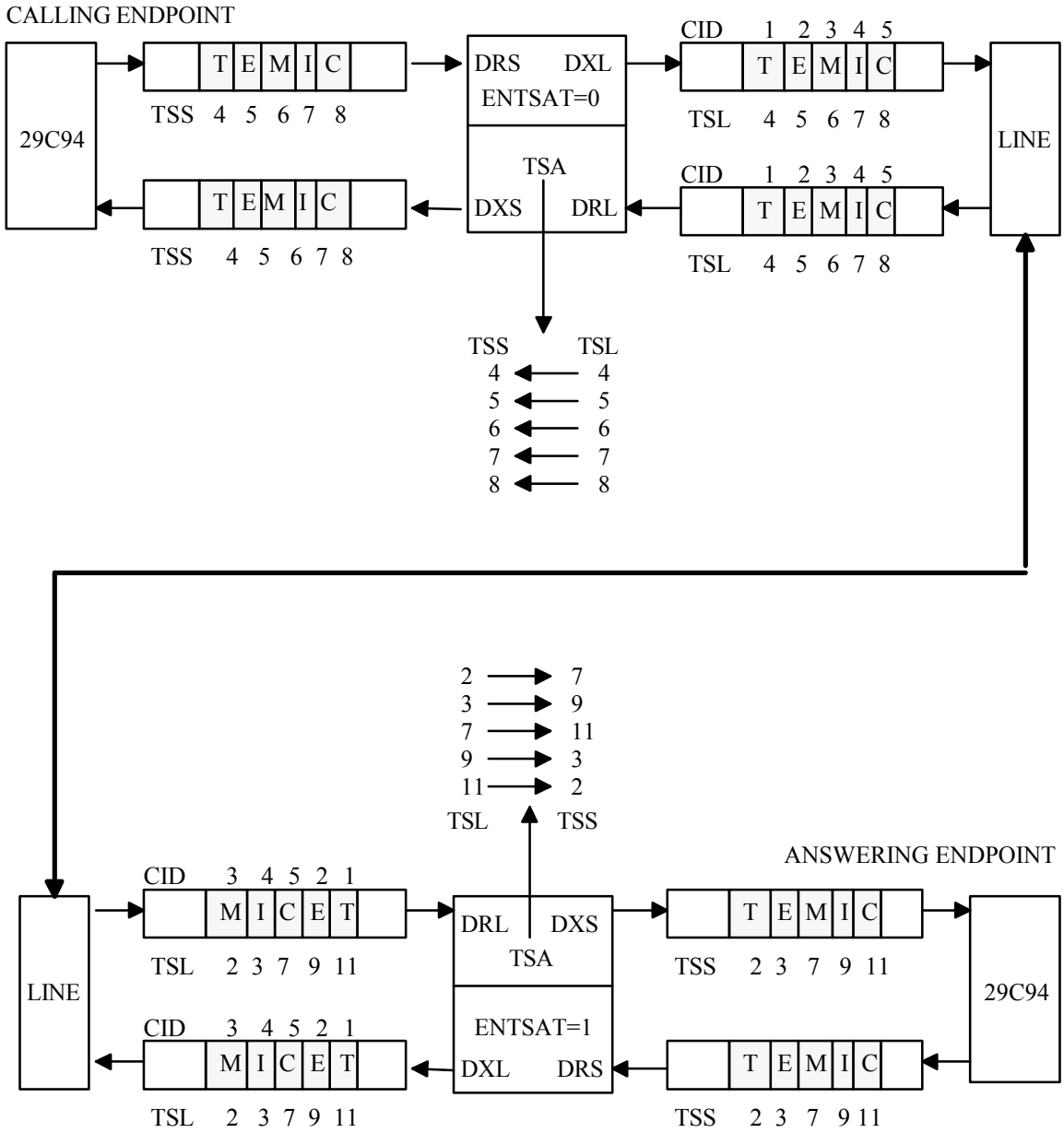
- "T" sent in channel with CID = 1,
- "E" in channel with CID = 2,
- "M" in channel with CID = 3,
- "I" in channel with CID = 1,
- "C" in channel with CID=2, etc....

Note : The CID are written by the µP in the TIC memory.

The CIDs' order may differ from the physical time slot order depending on whether or not the time slot reordering is active and which is the initial (Master) channel. To interface with a 29C94 circuit it is recommended to respect the following rules :

- CALLING ENDPOINT
  - Transmitter side : choose as a Master Channel the channel with the lowest physical number and the remaining channels with CID that follow the physical order. Set bit ENTSAT=0 (disable time slot reordering)
  - Receiver side : time slot reordering is normally not necessary (receive TSL = transmit TSL). Otherwise, update the register TSA with the corresponding TSS number.
- ANSWERING ENDPOINT
  - Receiver side : if a time slot reordering is necessary, update the register TSA with the corresponding TSS number.
  - Transmitter side : enable the time slot reordering (bit ENTSAT=1).

Figure 14. CIDs' choice



Microprocessor interface

The 29C98 has a "general purpose" µP interface bus :

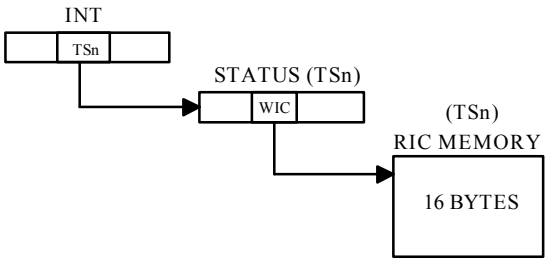
- 11 bit address bus
- 8 bit data bus
- $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RDY}$, $\overline{INTREQ}$, $\overline{RESET}$ command signals

Interrupt management

In order to follow the successive states of the BONDING algorithm, the µP will have to answer to interrupt requests from the 29C98. The interrupt process is organized into 3 stages :

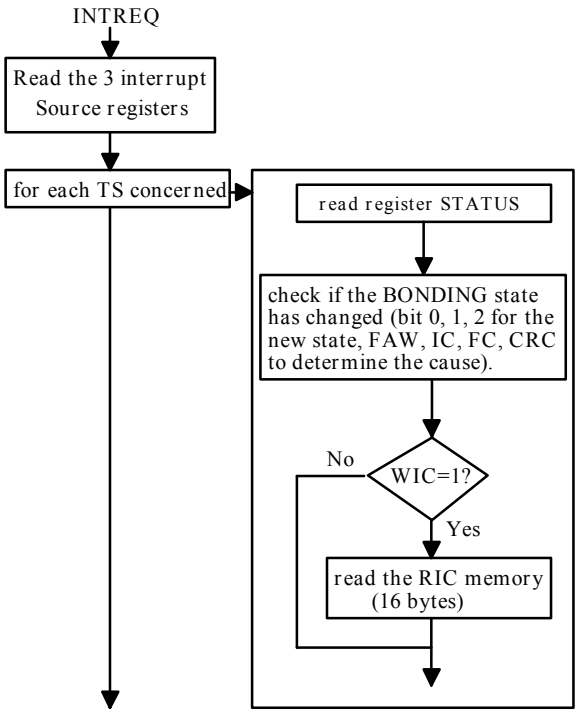
- Interrupt Source (INT) registers to determine the TS concerned,
- Receiver Channel Status (RSTAT) to report the current state in the BONDING process,
- Receiver IC (RIC) memory to report a write in the information channel memory.

Figure 15. Interrupt management : source of the interrupt signal



When an interrupt signal occurs, the µP has to perform the following actions :

Figure 16. Interrupt process



When read, the 3 Interrupt Source registers are cleared. So are the bits 3 to 7 of the Receive Channel Status register (RSTAT : bits WIC, CRC, FC, IC, FAW).

Hardware / Software Reset

In addition to the hardware Reset, three different software Reset modes are possible through the register RESET. In all the cases, the µP shall wait the end of the initialization process (2 x 512 x MCLK) before trying to read or write the 29C98.

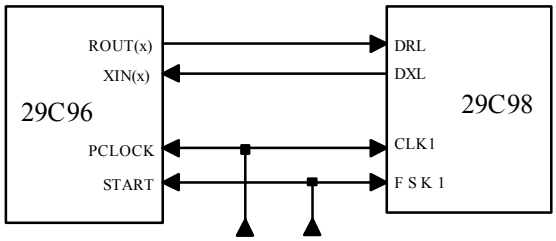
System architecture

Interface with the framer

The interface with a framer like the MATRA M.H.S. 29C96 is made up with :

- DRL, DXL : serial data link bus
- CLK1 : bit clock
- FSK1 : frame clock

Figure 17. Framer interface



(x) = 0, 1, 2 or 3

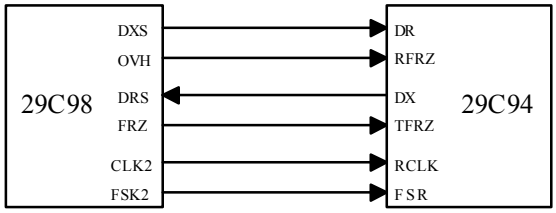
The data on DRL and DXL should be organized as time slots (2 up to 32) . The frequency on CLK1 is fixed to 1.544 Mb/s (T1/DS1) or 2.048 Mb/s (CEPT). It is possible to connect devices that handle only two time slots (i.e. a Basic access device like the 29C93A (Terminal Rate Adapter Circuit or TRAC)) only if the bit clock rate is 1.544 Mb/s or 2.048 Mb/s.

Interface with the protocol controller

The interface with the protocol controller is similar to the one of the framer :

- DRS, DXS : serial data link bus
- CLK2 : bit clock
- FSK2 : frame clock
- OVS, FRZ : inhibit receive/transmit

Figure 18. Protocol controller interface

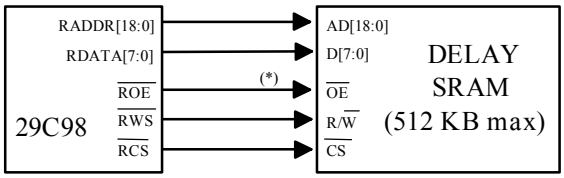


External delay RAM

The 29C98 includes 64 DMA channels (32 to write the data, 32 to read them) and interfaces with the external delay SRAM using a dedicated bus with the lines described below :

- 19 bit address bus
- 8 bit data bus
- $\overline{ROE}$, $\overline{RWS}$, $\overline{RCS}$, $\overline{RBUSY}$ command lines

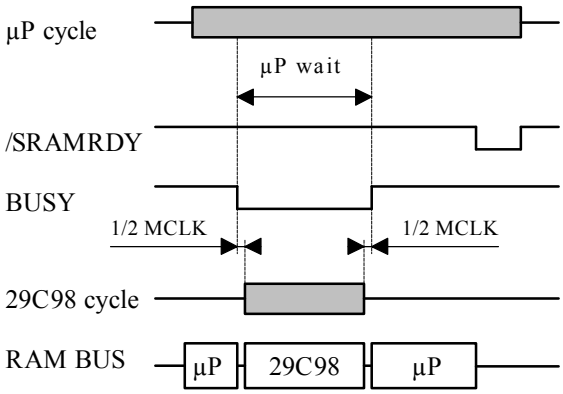
Figure 7. External delay RAM interface



(*) depends on the type of memory

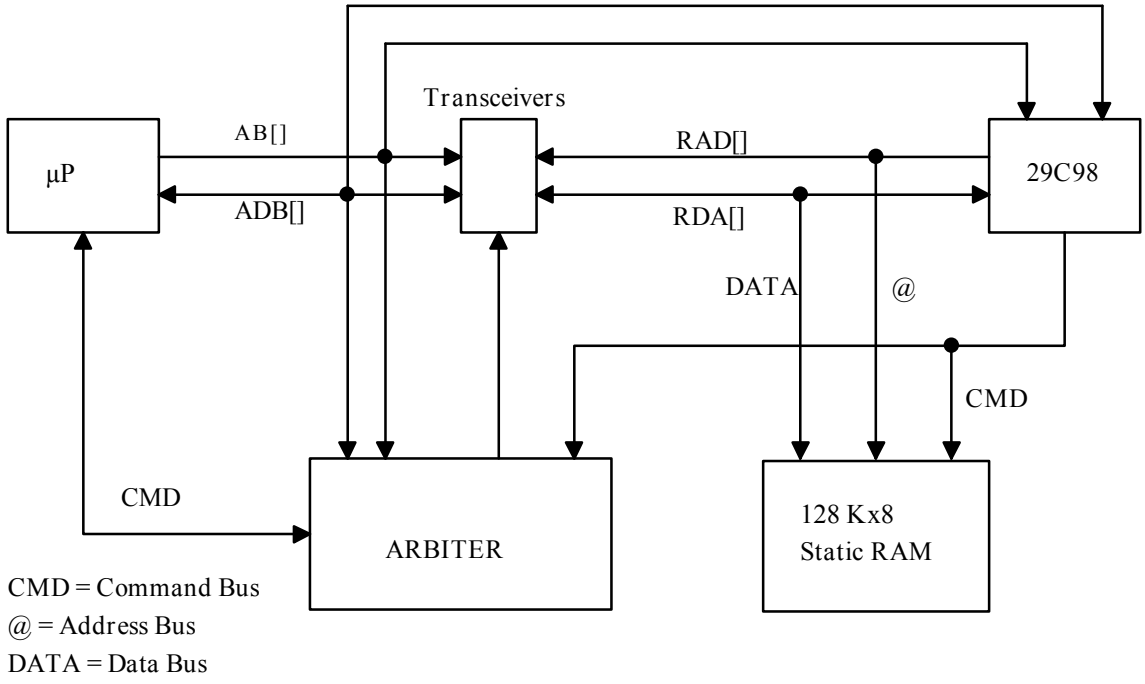
This memory can be shared by multiple master devices only if the 29C98 has the highest priority (the 29C98 read and write operations cannot be delayed). To enable the µP to read and write the Delay memory (self test purpose for example), the signal $\overline{RBUSY}$ shall be used by an external arbiter. When this signal becomes active (low), the arbiter shall ask the µP to release the buses as soon as possible (< 1/2 MCLK) (see timing diagram).

Figure 20. Example of a µP cycle interrupted by a 29C98 cycle



In the implementation example shown hereafter, transceivers are used to separate the µP bus and the 29C98 delay RAM bus. The arbiter checks continuously the $\overline{RBUSY}$ line from the 29C98. When it becomes active (low), the arbiter disables the transceivers. In addition, the arbiter shall manage a

Figure 21. Delay RAM access - example of implementation

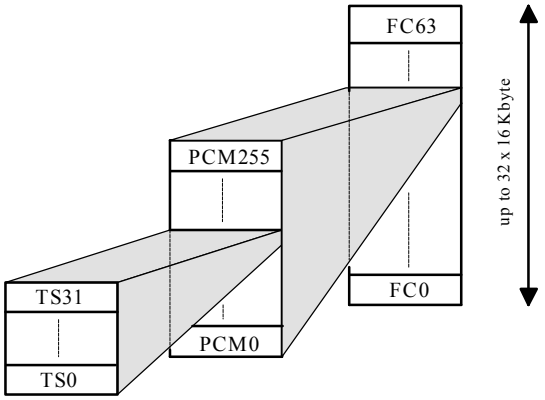


ready signal (/SRAMRDY) to delay the end of a µP cycle when is interrupted by the 29C98.

It is possible to choose the size of the external Delay RAM depending on the maximum acceptable delay between the fastest and the slowest channel of a call. The minimum value corresponds with a delay lower than a PCM frame duration : 32 Bytes (125 µs). As an example, for a delay lower than a BONDING frame duration, the amount of memory required is :

256 (number of PCM frames to carry one BONDING frame) x 32 (maximum TS number per PCM)
= 8 KByte (equivalent to 32 ms).

Figure 22. External Delay RAM organization



Register set

R/W : Read and Write register
R : Read only register
W : Write only register

NAME	ADDRESS	DESCRIPTION	TYPE	RESET
RIC	0 - 1FFh	Receive Information Channel Memory (0 - 31)	R/W	0
TIC	200h - 3FFh	Transmit Informmation Channel Memory (0 - 31)	R/W	0
RSTAT	400h - 41Fh	Receive status registers (0 - 31)	R	0
RCON	400h - 41Fh	Receive control registers (0 - 31)	W	0
TCON	420h - 43Fh	Transmit control registers (0 - 31)	R/W	0
INT	440h - 443h	Interrupt Source registers (0 - 3)	R	0
MASK	444h - 447h	Interrupt mask registers (0 - 3)	W	0
GLOBAL	448h	Global register	R/W	0
RESET	449h	Reset register	R/W	0
BCR	460h - 47Fh	Byte Count register for Read operation in the delay RAM (0 - 31).	R/W	0
FCR	480h - 49Fh	Frame Count register for Read operation in the delay RAM (0 - 31)	R/W	0
TSA	4A0h - 4BFh	Time Slot Allocation register for read operation in the delay RAM (0 - 31)	R/W	0
BCW	4C0h - 4DFh	Byte Count for Write operation in the delay RAM(0 - 31)	R/W	0
FCW	4E0h - 4FFh	Frame Count register for Write operation in the delay RAM(FC, 0 -	R/W	0

In the following, TSL will refer to a time slot number on the line side.
When T1/DS1 mode is selected, replace (0-31) by (0-23) and (0-3) by (0-2)

MSB RIC @ = 0h + 16xTSL RESET = 0 (R/W) LSB

	B7*	B6**	B5	B4	B3	B2	B1	B0**
Octet 1						NCRC	A	E
2	1	CHANNEL ID (CID)						1
3	1	GROUP ID (GID)						1
4	1	OPERATING MODE						1
5	1	RMULT						1
6	1				BCR		MFG	1
7	1	RI	RL REQ	RL IND	REV			1
8	1	SUBADDRESS						1
9	1	TRANSFER FLAG						1
10	1	1	DIGIT - 1					1
11	1	1	DIGIT - 2					1
12	1	1	DIGIT - 3					1
13	1	1	DIGIT - 4					1
14	1	1	DIGIT - 5					1
15	1	1	DIGIT - 6					1
16	1	1	DIGIT - 7					1

* Bit 7 received is not forced by the 29C98. The value written in the RIC corresponds to the received value. This bit shall be received equal to 1 with 64 kb/s bearer rate channels. With 56 kb/s channels, it is used for network signaling (=1 for off-hook).

** Bit 0 and bit 6 are not forced by the 29C98. They shall be received equal to 1 (Bonding standard).

OCTET 1 :

E : bit of the CRC byte (256 th byte of the BONDING frame). E=1 is received when the Remote End has detected a CRC4 error.

A : bit of the CRC byte (256 th byte of the BONDING frame). A=1 is received when the Remote End is not aligned on the Bonding frame.

NCRC : indication that the CRC4 procedure is not supported by the Remote End. This bit is set to 1 when the 29C98 detects three consecutive '1111' sequence in the CRC4 field, with a bit E set to 0 (no CRC4 error). The user shall disable the CRC4 procedure.

OCTET 2 to 16 : bytes received in the Information Channel (as defined in the BONDING standard).

TIC @ = 200h + 16xTSL RESET = 0 (R/W)

	MSB B7*	B6	B5	B4	B3	B2	B1	LSB B0*
Octet 1				CRC4				1
2	1	CHANNEL ID (CID)						1
3	1	GROUP ID (GID)						1
4	1	OPERATING MODE						1
5	1	RMULT						1
6	1				BCR		MFG	1
7	1	RI	RL REQ	RL IND	REV			1
8	1	SUBADDRESS						1
9	1	TRANSFER FLAG						1
10	1	1	DIGIT - 1					1
11	1	1	DIGIT - 2					1
12	1	1	DIGIT - 3					1
13	1	1	DIGIT - 4					1
14	1	1	DIGIT - 5					1
15	1	1	DIGIT - 6					1
16	1	1	DIGIT - 7					1

* Bit 0, 6 and 7 are forced to 1 by the 29C98 as indicated.

OCTET 1 :
CRC4: current value of the CRC4 field of the BONDING CRC word (256 th byte of the BONDING frame). This field shall not be modified (read only).

OCTET 2 to 16 : bytes to transmit in the Information Channel (as defined in the BONDING standard).

MSB RSTAT @ = 400h+TSL RESET = 0 (R) LSB

7	6	5	4	3	2	1	0
FAW	IC	FC	CRC	WIC	CODE		

CODE	State	Mode	Description
0 0 0	OOS	All	Out of synchronization
0 0 1	ICFF	0,1,2	Master IC alignment found
0 1 0	ICFVAL	0,1,2	Master IC data valid
0 1 1	FAWF	1,2	FAW alignment found
1 0 0	ICSF	1,2	IC alignment found
1 0 1	ICSVAL	1,2	IC valid
1 1 0	GTG	0,1,2	Ready for data transfer
1 1 1	RUNX	Ext	Run with external synchronization

WIC: set to 1 when a new data has been received in the RIC memory
CRC: set to 1 when a bad CRC4 has been received (mode 2 only)
FC: set to 1 when the FC field has not been received in sequence
IC: set to 1 when the IC frame synchronization has been lost (3 consecutive frames)
FAW: set to 1 when the Bonding multiframe synchronization has been lost (3 consecutive multiframes)

MSB RCON @ = 400h+TSL RESET=0 (W) LSB

7	6	5	4	3	2	1	0
				CODE			

CODE	State	Mode	Description
0 0 0 0	TRSP	All	Waiting for a call connection
0 0 0 1	ICFS	0,1,2	Search Master channel
0 0 1 0	FAWS	1,2	Search for FAW alignment
0 0 1 1	-	-	not used
0 1 0 0	RUNN	0,1,2	Enable data reception
0 1 0 1	FAWAD	2	Add channel to an existing call
0 1 1 0	XSY	Ext	External synchronization
0 1 1 1	-	-	Not used
1 0 1 0	FAWCS	1, 2	Search FAW alignment with CRC4
1 0 1 1	-	-	Not used
1 1 0 0	RUNC	2	Enable data reception with CRC4
1 1 0 1	FAWADC	2	Add channel with CRC4

MSB TCON @ 420h+TSL RESET=0 (R/W) LSB

7	6	5	4	3	2	1	0
		A	E	CODE			

CODE	State	Mode	Description
0 0 0 0	TRSP	-	Transparent
0 0 0 1	ICT	0,1,2	Transmit Master channel (full bandwith = 64 Kb/s)
0 0 1 0	FAWT	1,2	Transmit Bonding multiframe (FAW alignment)
0 0 1 1	RUNN	0,1,2	Enable data transfer without CRC4
0 1 0 0	RUNC	2	Enable data transfer with CRC4
0 1 0 1	LOOP	2	Remote loop back
0 1 1 0	ONES	-	Transmit an all 1's pattern
0 1 1 1	HIZ	-	Channel in High impedance
1 0 1 0	FAWTC	1,2	Transmit Bonding multiframe (FAW alignment) with CRC4 enabled
1 1 0 1	LOOPC	2	Remote loop back with CRC4

E: bit of the CRC byte (256 th byte of the BONDING frame). Used to indicate to the Remote End an error on the received CRC4 (E=1).

A: bit of the CRC byte (256 th byte of the BONDING frame). Used to indicate to the Remote End the synchronization on the Bonding frame is achieved (A=1).

MSB INT0 @ = 440h RESET = 0 (R) LSB

7	6	5	4	3	2	1	0
IT7	IT6	IT5	IT4	IT3	IT2	IT1	IT0

MSB INT1 @ = 441h RESET = 0 (R) LSB

7	6	5	4	3	2	1	0
IT15	IT14	IT13	IT12	IT11	IT10	IT9	IT8

MSB INT2 @ = 442h RESET = 0 (R) LSB

7	6	5	4	3	2	1	0
IT23	IT22	IT21	IT20	IT19	IT18	IT17	IT16

MSB INT3 @ = 443h RESET = 0 (R) LSB

7	6	5	4	3	2	1	0
IT31	IT30	IT29	IT28	IT27	IT26	IT25	IT24

IT0 to IT31 : when set to 1, indicates the channels which have caused the interrupt pin to become active. The interrupt pin remains active until all the registers that contain a bit set to 1 are read.

MSB MASK0 @ = 444h RESET = 0 (R/W) LSB

7	6	5	4	3	2	1	0
EIT7	EIT6	EIT5	EIT4	EIT3	EIT2	EIT1	EIT0

MSB MASK1 @ = 445h RESET = 0 (R/W) LSB

7	6	5	4	3	2	1	0
EIT15	EIT14	EIT13	EIT12	EIT11	EIT10	EIT9	EIT8

MSB MASK2 @ = 446h RESET = 0 (R/W) LSB

7	6	5	4	3	2	1	0
EIT23	EIT22	EIT21	EIT20	EIT19	EIT18	EIT17	EIT16

MSB MASK3 @ = 447h RESET = 0 (R/W) LSB

7	6	5	4	3	2	1	0
EIT31	EIT30	EIT29	EIT28	EIT27	EIT26	EIT25	EIT24

EIT0 to EIT31 : when set to 1, enables the corresponding interrupt bit (ITxx) to generate an interrupt. When reset to 0, the associated interrupt bit will never generate an interrupt (bit ITxx masked).

MSB GLOBAL @ = 448h RESET = 0 (R/W) LSB

7	6	5	4	3	2	1	0
CLRT	ENDXS	ENTSAT	ENDXL	TRIGX	TRIGG	ENFBIT	MODE

The register called GLOBAL is used to perform commands that concern the whole circuit :

MODE: selects E1(0) or T1 (1) PCM format (32 or 24 time slots)

ENFBIT: only with MODE=1 (T1)
When set to 1 : enables the 193rd bit (F) of the frame to be transmitted unchanged
When reset to 0 : the bit F is not transmitted (High impedance) towards the line and towards the system

TRIGG: Toggle bit used to start / stop synchronously the counters FCR / BCR (DMA read) for all the time slots marked with bit SSCNT=1 (normally of the same group). This bit is used for relative delay computation (the counters are stopped) and to enable the data transfer (the counters are enabled).

TRIGX: Toggle bit used to start / stop the counters FCW / BCW (DMA write) for all the time slots of the same group (marked with XSY). With external equalization only (the relative delays are determined outside the 29C98).

ENDXL: when set to 1, enables the PCM line DXL
When reset to 0, DXL is in high impedance.

ENTSAT: enables the Timeslot Allocation Table for transmission (system side towards line side).

ENDXS: when set to 1, enables the PCM line DXS
When reset to 0, DXS is in high impedance.

CLRT: clear internal Tags. Must be clear to 0 in normal use.

MSB RESET @ = 449h RESET = 0 (W) LSB

7	6	5	4	3	2	1	0
					TRS	RCV	GLOB

GLOB: when set to 1, the component is reset as with the hardware signal (all registers and state machines are concerned). The µP must not try to access the chip before 6*512*MCLK after having written GLOB=1.

RCV: when set to 1, the receiver part of the circuit is reset (RIC memory + RCON + RSTAT + state machines). The µP must not try to access the chip before 6*512*MCLK after having written RCV=1.

TRS: when set to 1, the transmitter part of the circuit is reset (TIC memory + TCON + state machines). The µP must not try to access the chip before 6*512*MCLK after having written TRS=1.

MSB BCR @ = 460h+TSL RESET =0 (R/W) LSB

7	6	5	4	3	2	1	0
O to 255							

BCR : 8 bit register (0 to 255). Receiver Byte Count. This register is incremented by 1 every PCM frame. It shall be initialized before data transfer is enabled In Bonding mode 1, 2 and with external equalization (is a part of the address used to read the delay RAM : bit 5 to 12).

MSB FCR @ = 480h+TSL RESET =0 (R/W) LSB

7	6	5	4	3	2	1	0
		0 to 63					

FCR : 5 bit register (0 to 63). Receiver Frame Count. This register is incremented by 1 every Bonding multiframe (256 PCM frame). It shall be initialized before data transfer is enabled In Bonding mode 1, 2 and with external equalization (is a part of the address used to read the Delay RAM : bit 13 to 19).

MSB TSA @ = 4A0h+TSS RESET =0 (R/W) LSB

7	6	5	4	3	2	1	0
LOOP	SSCNT	ENTS	TSL				

TSL: TSL is the time slot number (0 to 31) on Line side (framer side) associated to the current time slot on the system side (TSS). If TSS different than TSL, time slot number TSS is no more available on the line side.

ENTS: when set to 1, the time slot (TSS on system side) is enabled. If reset to 0, the time slot is not driven (High impedance).

SSCNT: start / stop counters. This bit is a toggle bit. Used with TRIGG (register GLOBAL), it enables or disables counter FCR, BCR for this time slots.

LOOP: enables the Remote loop back feature (DXS internally connected with DRS). The incoming time slot TSL is looped back in the outgoing time slot TSL. The Remote Loopback feature is only available for Mode 2 with the 29C98.

MSB BCW @ = 4C0h+TSL RESET =0 (R/W) LSB

7	6	5	4	3	2	1	0
O to 255							

BCW : 8 bit register (0 to 255). Transmitter Byte Count. This register is incremented by 1 every PCM frame. It shall be initialized before data transfer is enabled with external equalization (is a part of the address used to write the delay RAM : bit 5 to 12).

MSB FCW @ = 4E0h+TSL RESET =0 (R/W) LSB

7	6	5	4	3	2	1	0
		0 to 63					

FCW : 5 bit register (0 to 63). Transmitter Frame Count. This register is incremented by 1 every Bonding multiframe (256 PCM frame). It shall be initialized before data transfer is enabled with external equalization. Is a part of the address used to write the Delay RAM : bit 13 to 19).

Operating sequences

Conventions

TS = Time Slot or Channel
µP = microprocessor
DN = Directory number

ICF = "Fast" information Channel (Master)
FAW= Bonding Multiframe
ICS = "Slow" information Channel

NF = no framing
- = not applicable

In the following, we first will consider an equipment (the Caller or Calling Endpoint) that wants to establish a wideband communication according to the BONDING specification in mode 0, 1 or 2. The following table summarizes the main actions that must be taken to handle the protocol.

We suppose the Caller has established a connection using the channel D (or other means). This first connected channel (TS) will be used as the MASTER channel (TS_{Master}) for negotiating the parameters of the Call.

Action	mode 0	mode 1	mode 2
Initial Channel setup / Initiate a Master Channel	ICF	ICF	ICF
Negotiation of the Call (Master Channel)	ICF	ICF	ICF
Directory number exchange (Master Channel)	ICF	ICF	ICF
End of negotiation process (Master Channel)	ICF	ICF	ICF
Establisment of BONDING multiframe (Master Channel)	-	FAW + ICS	FAW + ICS
Additional Channel setup	-	FAW + ICS	FAW + ICS
Relative delay calculation	-	FAW + ICS	FAW + ICS
Delay equalization	-	FAW + ICS	FAW + ICS
Timeslot reordering	NF	FAW + ICS	FAW + ICS
Switch Master Channel to data transfer	NF	NF	FAW + ICS
Switch ddditionnal Channels to data transfer	NF	NF	FAW + ICS
Negotiation of additionnal Bandwidth	-	-	FAW + ICS
Add a new channel to an existing Call	-	-	FAW + ICS
Deleting Bandwidth	-	-	FAW + ICS
External synchronization	-	-	-

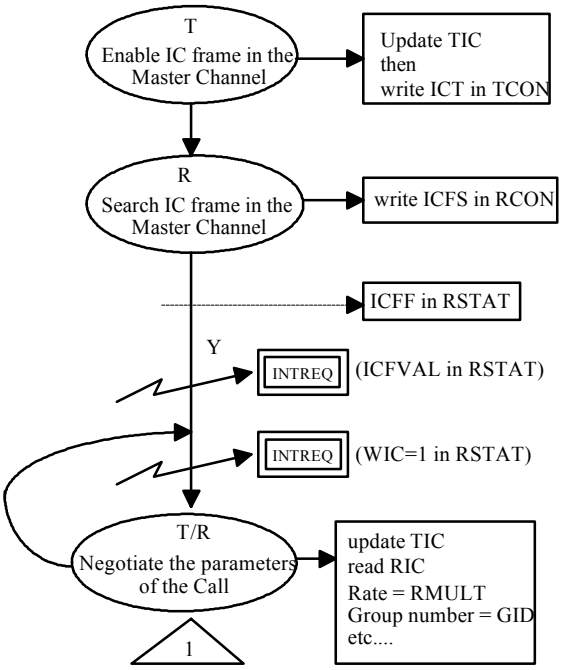
In the following, the flow charts will include the symbols defined below :

Initial Channel setup / Initiate a Master Channel (mode 0, 1, 2) (figure 23)

To use a Channel as the Master Channel of a new Call, the µP will have to program :

- RECEIVER SIDE : the register RCON (@400h + TS_{Master} , lower nibble) with the code field = ICFS (search for Master Channel).
- TRANSMITTER SIDE : the TIC Memory of TS_{Master} (@200h + 16xTS_{Master}) shall first be filled with parameters that define the features of the communication link to establish (number of TS, mode of operation etc...). These parameters will be negotiated with the Remote End. Then the register TCON (@420h + TS_{Master} lower nibble) shall be written with the code field = ICT (Transmit Master Channel). This will enable the transmission of an IC frame using the whole Bandwidth (64 kb/s).

Figure 23. Initiate Master channel l- negotiation of the parameters (MODE 0, 1, 2)



Negotiation of the Call (mode 0, 1, 2) (figure 23)

The negotiation of the parameters of the Call can begin only when each end detects the synchronization of the IC.

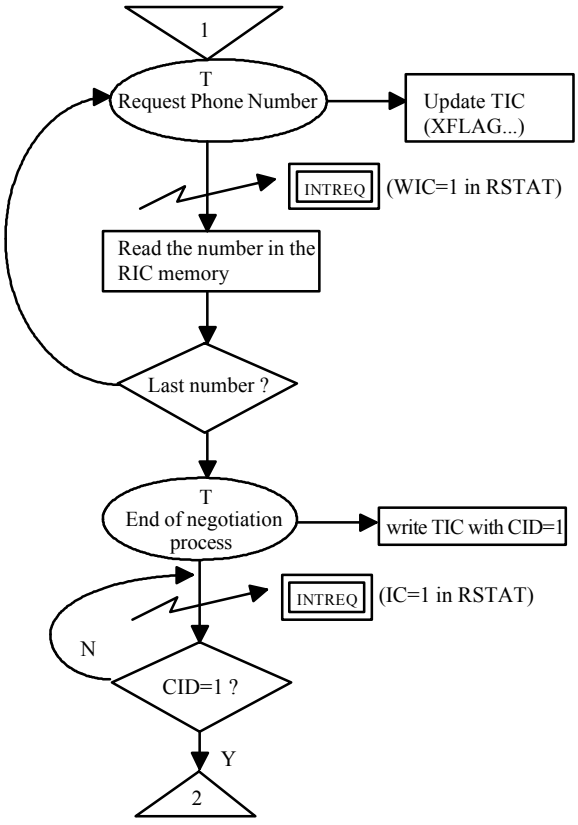
- RECEIVER SIDE : When the 29C98 is locked on the IC, the code in the corresponding register RSTAT (@400h + TS_{Master}) indicates ICFF (no interrupt signal). An interrupt is generated when the values in the RIC memory are valid (code ICFVAL in register RSTAT). New negotiated values will then be received in the RIC memory and indicated by an interrupt (bit WIC=1 in register RSTAT).
- TRANSMITTER SIDE : parameters can be updated in the TIC memory by the µP during the negotiation phase.

Directory Number exchange (mode 0, 1, 2) (figure 24)

Once both ends agreed on the parameters of the communication link :

- TRANSMITTER SIDE : the Caller requests the phone numbers corresponding to the additional channels needed (field XFLAG in the TIC memory area).

Figure 24. Directory number exchange - End of parameter negotiation (Mode 0, 1, 2)



- RECEIVER SIDE : Each time a new phone number is received in the RIC memory, an interrupt is generated (bit WIC=1 in register RSTAT).

End of the negotiation process (mode 0, 1, 2)

- TRANSMITTER SIDE : when the last phone number has been received, the Caller indicates the conclusion of the negotiation process by writing CID=1 in the TIC memory.
- RECEIVER SIDE : When CID=1 is received in the RIC memory, the caller initiates the connection of the remaining channels (via channel D ...).

BONDING multiframe in the Master Channel (mode 1, 2)

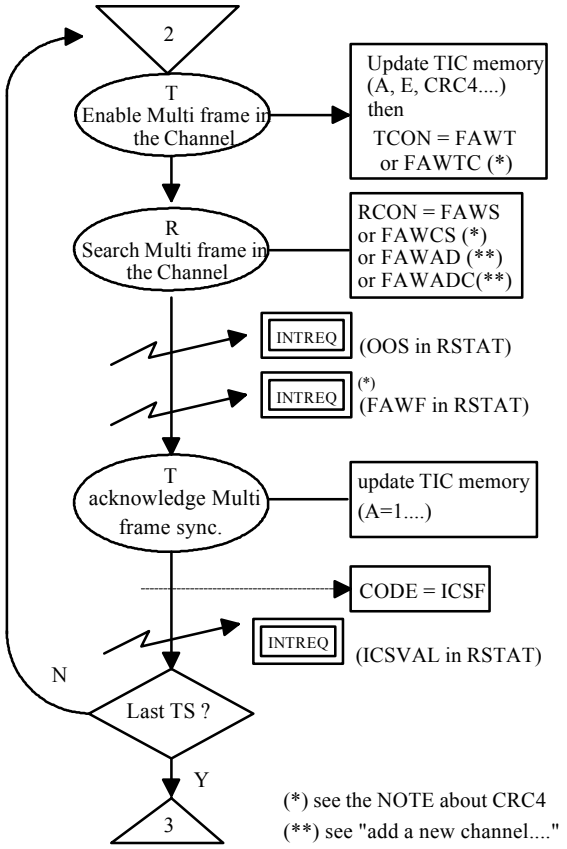
- TRANSMITTER SIDE : as the Caller receives CID=1, it updates the TIC memory (A, E, CRC4...) and starts transmitting the Bonding multiframe by writing FAWT or FAWTC (CRC4 generation enabled) in register TCON (for TS_{Master}).
- RECEIVER SIDE : the µP shall program the register RCON with code = FAWS (search for Bonding overall Frame alignment) or FAWCS (CRC4 enabled). the receiver will generate interrupts signal to indicate successively (in the register RSTAT of TS_{Master}) :
  - OOS because the Remote End switches from transmitting the IC to the Bonding multiframe,
  - FAWF when the synchronization on the overall BONDING frame is achieved,
  - ICSF when the IC synchronization is found (no interrupt) and
  - ICSVAL when 2 complete IC frames are received without changes.

NOTE ABOUT CRC4 : When the 29C98 founds the Multiframe alignment, it checks the CRC4 field. If an error is found, a CRC4 error is reported to the µP (bit CRC in register RSTAT). If the CRC4 field received matches with '1111' during 3 multiframes with E=0, the Remote End is supposed not supporting the CRC4 feature and an interrupt is also generated (WIC=1 in register RSTAT to indicate that the RIC memory has changed : NCRC=1 in the first byte).

Additional Channel setup (mode 1,2)

- TRANSMITTER SIDE : for each additional channel, when the connection is established, the Caller shall begin transmitting the multiframe structure. For each TS, the programming of the 29C98 and the steps to follow are the same as previously described for the Master channel (see flow chart "BONDING MULTIFRAME..", step 2). Take care in updating the TIC memory of each TS that, part of the information are common to all the TS (GID, RMULT....), and part of the information are dedicated to a single TS (CID ...).
- RECEIVER SIDE : if the new channel is added to an existing call (see "add a channel..."), the code in RCON shall be FAWAD (or FAWADC with CRC4 enabled) instead of FAWS (or FAWCS with CRC4 enabled). Each time a new valid IC is received, the µP shall read the information (GID, CID etc...) and check if all the channels of the call are synchronized.

Figure 25. Bonding Multiframe (MODE 1, 2)



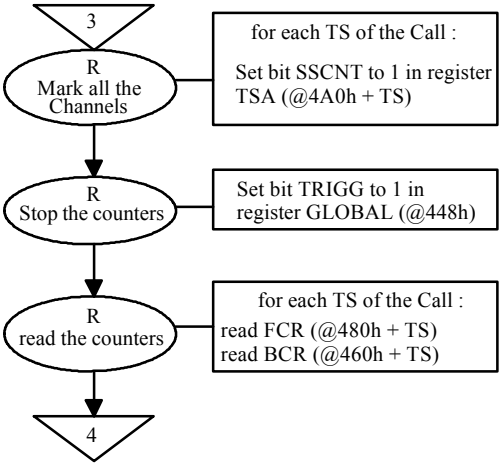
Relative delay calculation (mode 1, 2) (figure 26)

- RECEIVER SIDE : from the moment ICSVAL information has been received in one channel, FCW and BCW counters of this channel are copied in FCR / BCR until they are read for relative delay calculation. To have a maximum accuracy, the counters' content of all channels of the call must be stopped as the same time. The following steps must be followed :

  - mark all the TS concerned by writing SSCNT=1 (stop counter) in register TSA (@4A0h + TS),
  - write TRIGG=1 in register GLOBAL to stop the counters FCR / BCR on next FSK1 (frame start, acknowledged by TRIGG=0 when TSA is read back)

  To perform the measurement of the relative delay variance between the individual channels of the Call, the µP shall read the FCR (@480h + TS) and BCR (460h + TS) stable values.

Figure 26. Relative delay calculation (Mode 1,2)



Delay equalization (mode 1,2) (figure 27)

- RECEIVER SIDE : As FCW with BCW is used as pointer to write the Delay Ram, FCR (@480h to 49Fh) with BCR (@460h to 47Fh) is used as a pointer to read the Delay RAM.
  Once all the relative delays are known, we can initialize the FCR and BCR values following the steps below :

  - take the FCRs / BCRs values previously read of the slowest Channel,
  - write FCR / BCR of each Channel with : (256 * FCRs) + (BCRs - CID)

TS reordering (mode 0, 1, 2) (figure 27,28)

- RECEIVER SIDE : in some cases, it is necessary to reorder the TS :

  - mode 1 and 2 : to respect the order of the received CID (the CIDs should increase with the TS number for 29C94 protocol controller),
  - this feature is also available in mode 0 and is application dependent.

  The µP shall write register TSA in the following way (if $TSS_{(n+i)}$ should be sent before $TSS_{(n)}$) :

  - write (n+i) @ (4A0h + n)
  - write (n) @ (4A0h + n+i)

Figure 27. Delay equalization - Time slot reordering (Mode 1,2)

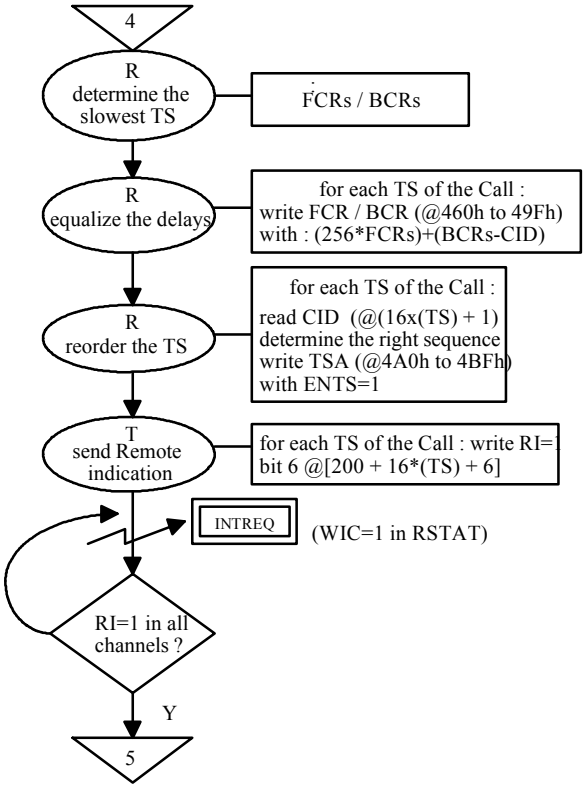
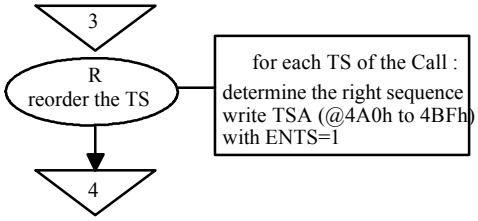


Figure 28. Time slot reordering (Mode 0)



Once all the channels are reordered and equalized, and before switch to data transfer :

- TRANSMITTER SIDE : The caller shall transmit the Remote Indication (RI=1) in the Information Message to the Remote End (write RI=1 in the TIC memory for all the TS of a single GID).

Switch Master Channel to data transfer in (mode 0) (figure 29)

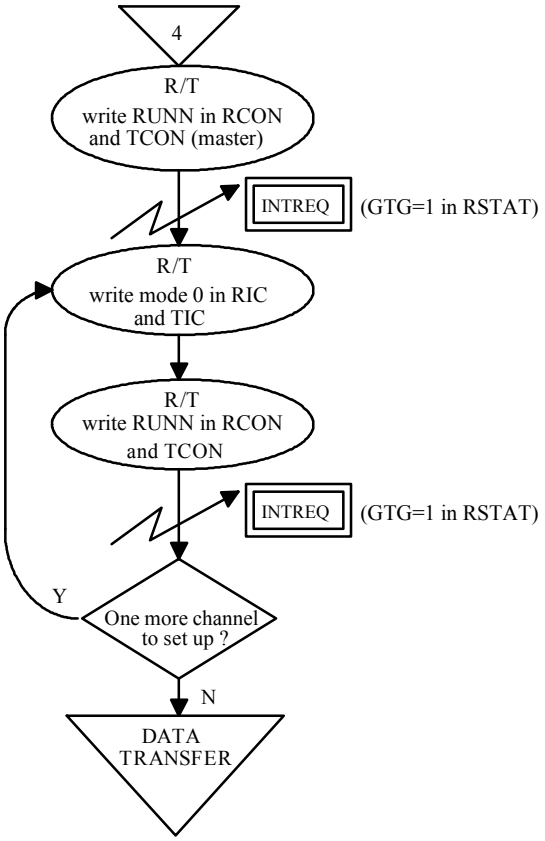
- RECEIVER SIDE : As soon as CID=1 is received in the RIC, we must write RUNN in the register RCON. An interrupt is then generated to acknowledge the RUNN command (code = GTG in register RSTAT). The desynchronization that appears in the master channel after the RUNN command does not generate an interrupt (the channel is treated as transparent).

- TRANSMITTER SIDE : the data transmission is selected (an enabled) by writing code = RUNN in register TCON.

Switch additional Channels to data transfer (mode 0) (figure 29)

Each time a new TS is connected, the µP has to program the operating mode 0 in the TIC and RIC, then RUNN in RCON and TCON as with the Master Channel (also acknowledged by code GTG) .

Figure 29. Switch channels to data transfer (Mode 0)



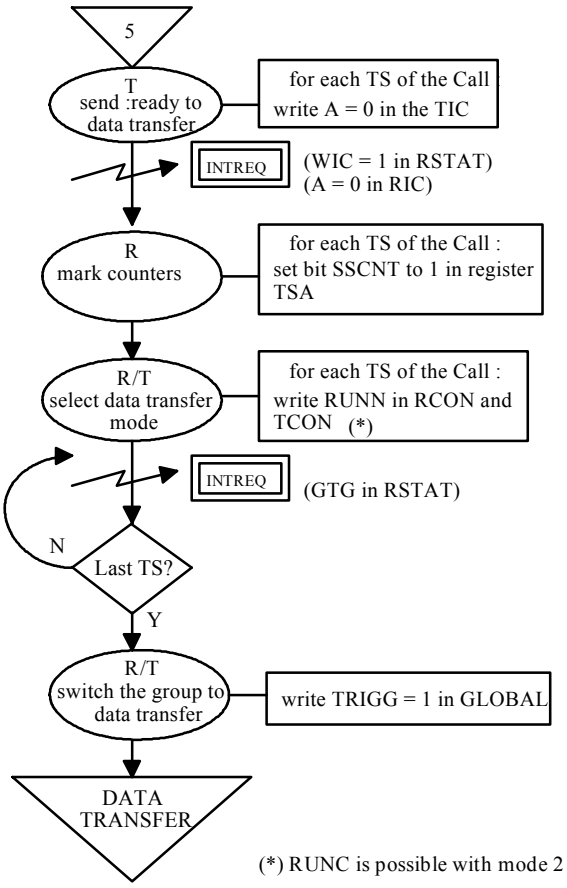
Switch to data transfer (mode 1, 2) (figure 30)

- RECEIVER SIDE : an interrupt shall occur with WIC=1 in register RSTAT for all channels of the call indicating that RI=1 has been received (Remote End equalized).
  The counters previously stopped to evaluate the relative delays must now be marked (SSCNT in register RCON of each TS) to be restarted synchronously (to generate the read address of the delay memory).
  The µP shall then write code = RUNN in register RCON of each TS of the Call (an interrupt caused by bit GTG gives an acknowledge)

- TRANSMITTER SIDE : The µP must write code = RUNN in register TCON of each TS of the Call.

Writing TRIGG=1 in register GLOBAL switches the Receiver and the Transmitter to data transfer (data valid on DXS) for the current GID (on the first following rising edge of FSK2).

Figure 30. Switch to data transfer (Mode 1, 2)



-

NOTE : in mode 2, code RUNC (with CRC4 feature enabled) may be written in RCON / TCON instead of code RUNN.

Negotiation of additional Bandwidth (mode 2) (figure 31)

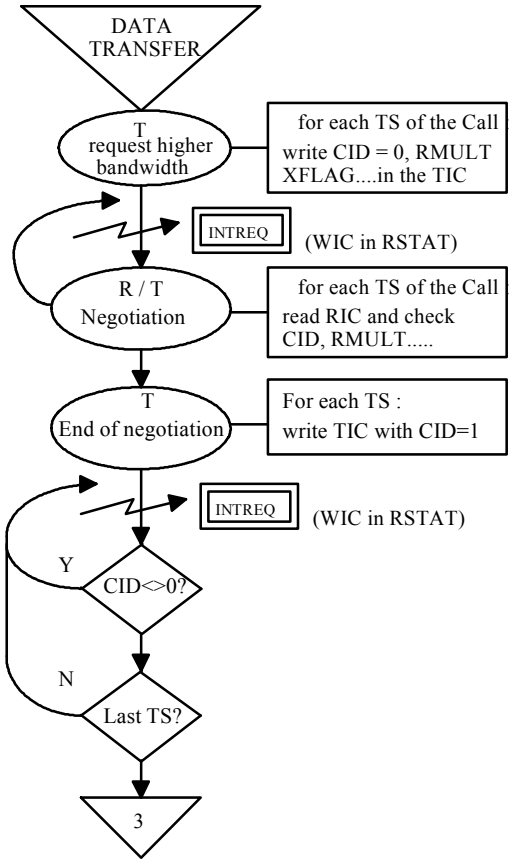
- TRANSMITTER SIDE : When the Calling Endpoint wants to set up additional bandwidth, it shall write the TIC memory (for all channels) with fields CID=0 (negotiation) and RMULT with the new value. Because in mode 2 at least one new channel is needed, the Caller shall also request a phone number for each additional channel (field XFLAG=1, then follow the procedure described earlier to transfer the phone numbers).

- RECEIVER SIDE : the request is accepted by the Remote End if CID=0 is received with all other parameters at the new requested values (interrupt caused by bit WIC=1 in register RSTAT for each new value received and each TS).

- TRANSMITTER SIDE : if the Remote End accepts the request (compare transmitted and received parameters), write CID = non-zero Identifier in the TIC memory for each channel.

- RECEIVER SIDE : when a CID=1 is received in the RIC memory (WIC=1 in RSTAT), the Calling endpoint initiates the connection of the new channel(s) using the received phone number(s).

Figure 31. Negotiation of additional bandwidth (Mode 2)



Add a new channel to an existing Call (mode 2)

Once the connection of the new TS is established :

- RECEIVER SIDE : write code = FAWAD in register RCON will start looking for BONDING multiframe and Information Channel alignment

(FAWADC with CRC4 enabled).

- TRANSMITTER SIDE : initialize the TIC memory (fields A, E, CID ...) then write code = FAWT or FAWTC (CRC4 generation enabled) in register TCON to enable the transmission of the BONDING multiframe with a valid IC.

- RECEIVER SIDE : as for the initial channels of the call we will have the following status for the new TS:

  - FAWF when the synchronization on the overall BONDING frame is achieved,
  - ICSF when the IC synchronization is found and
  - ICSVAL when 2 complete IC frames are received without changes.

Then a change in the RIC memory should be reported that correspond to a reception of A=1 (Remote End synchronized).

Enable data transfer (mode 2) (figure 32)

Once all the channels of a call have received the status ICSVAL, we must follow the procedure explained earlier (step 3 up to the data transfer) :

- relative delay calculation
- delay equalization
- Time slot reordering
- switch to data transfer

Deleting Bandwidth (mode 2)

- TRANSMITTER SIDE : When the Calling Endpoint wants to reduce the bandwidth, it shall write the TIC memory (for all channels) with fields CID=0 (negotiation) and RMULT with the new value.
  If only one channel has to be deleted, the Caller shall write field XFLAG with the CID of the corresponding Time slot. Otherwise, the channels with the higher CID will be deleted.

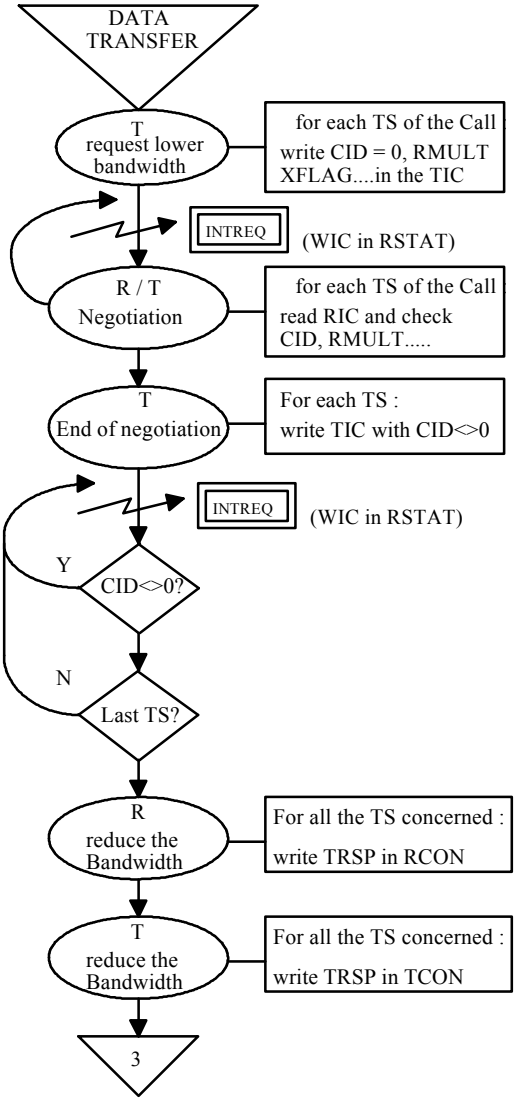
- RECEIVER SIDE : first, CID=0 is received as an acknowledgment followed by the new parameters of the call (indicating that the changes are accepted by the Remote End).

- TRANSMITTER SIDE : the CIDs are changed to non zero values in the TIC.

- RECEIVER SIDE : non zero CIDs are received indicating the end of the negotiation. We must write code = TRSP in register RCON for the channel(s) to be deleted. Then, if necessary, we may have to equalize the delays and a new sequence of Channel identifiers may be received.

- TRANSMITTER SIDE : we must write code = TRSP in register TCON to disable the Channel. If necessary, we may have to equalize the delays and resequence the Channel identifiers.

Figure 32. Deleting Bandwidth (Mode 2)



Enable data transfer (mode 2)

If all the remaining channels of the call stayed with the status ICSVAL in RCON, we can follow the procedure explained earlier (step 3 up to the data transfer) :

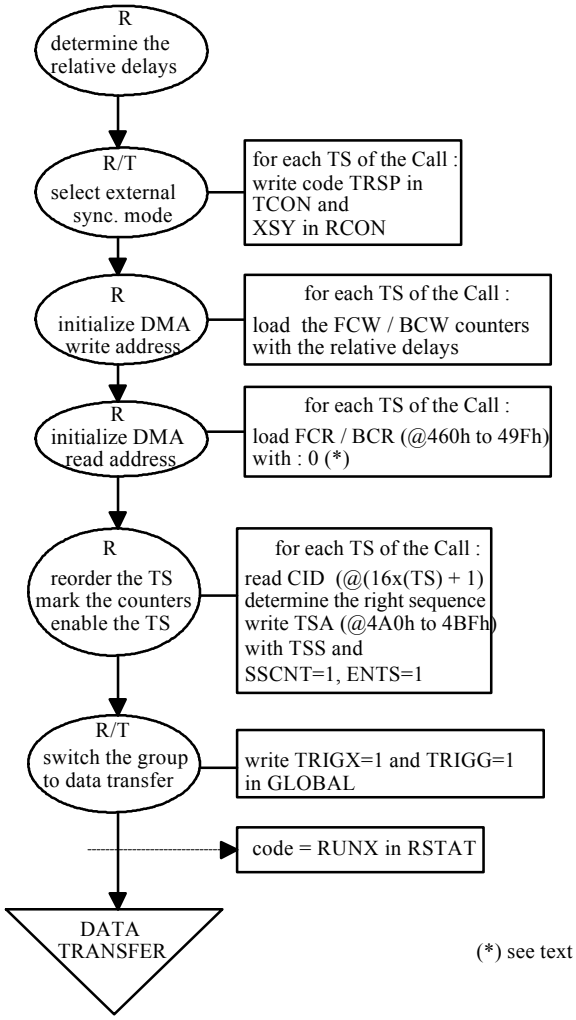
- relative delay calculation (if needed)
- delay equalization (if needed)
- Time slot reordering (if needed)
- switch to data transfer

External synchronization (figure 33)

The 29C98 is able to perform the delay equalization on channels that do not carry Bonding information (in that case,the relative delay measurements must be done with some other means).

- RECEIVER SIDE : To program the external synchronization mode, code XSY shall be written in register RCON of all the channels of the call When all the relative delays are known, they shall be used to initialize FCW / BCW counters (the counters can be initialized to 0 for the slowest channel. The remaining counters are loaded with the delay of the channel relative to the slowest channel). Then it is necessary to initialize the FCR / BCR counters. If no extra information are included inside the incoming data stream, all counters can be initialized with the same value chosen for the slowest channel (for example 0). The bits SSCNT and ENTS must be set to 1 in the register TSA to mark the counters to be started and to enable the transmission of this time slot towards the system side (a time slot reordering is also possible at this step). Once all the counters have been initialized, they must be turned on by setting bit TRIGX and TRIGG (in GLOBAL) to 1 (the state of the receiver changes from OOS to RUNX in RSTAT).
- TRANSMITTER SIDE : the external synchronization mode is selected by writing code TRSP in register TCON.

Figure 33. External synchronization



Electrical Characteristics

Absolute Maximum Ratings

VCC to GND ..... -0.5 V to +7 V
Input/Output Voltage .....-0.3 V to VCC + 0.3 V
Storage Temperature ..... -65 to 150 °C

Operating Conditions

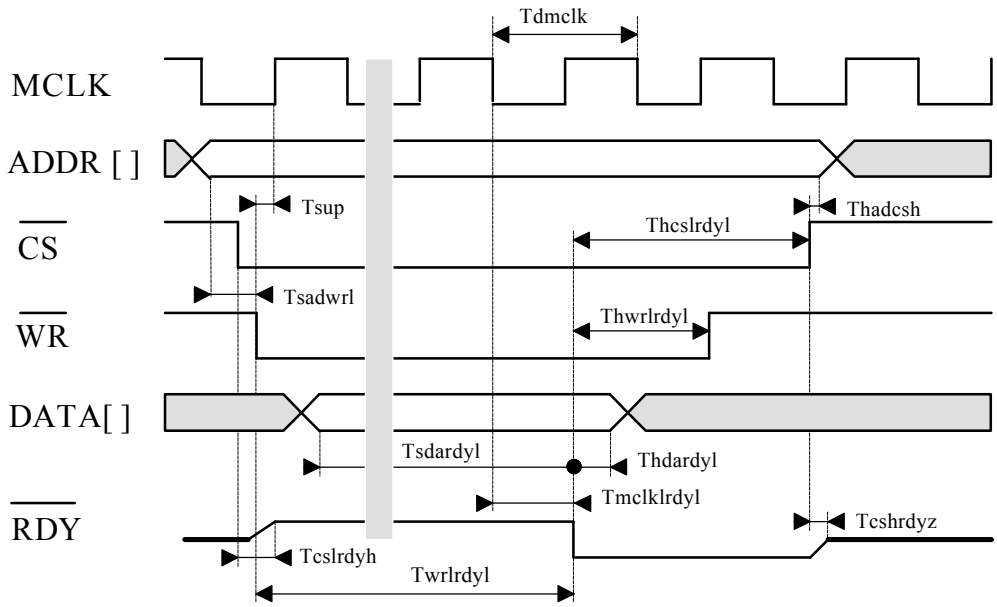
Voltage Range ..... 4.5 V to 5.5 V
Temperature range (commercial) ..... 0 to 70 °C
Temperature range (industrial)..... -40 to 85 °C

DC Electrical Characteristics (0°C - 70°C)

Parameter		Conditions	Min	Max	Unit
Low level input voltage	VIL	I = 5 µA		0.8	V
High level input voltage	VIH	I = 5 µA	2.2		V
input leakage current	Ileak			5	µA
3 state output leakage current	IOL			10	µA
low level output voltage	VOL	I = -6.4 mA		0.4	V
high level output voltage	VOH	I = 6.4 mA	2.4		V
standby current	ICCS	VCC = 5.5 V		200	µA
operating current	ICCOP	VCC = 5 V, 20 MHz Clock		100	mA

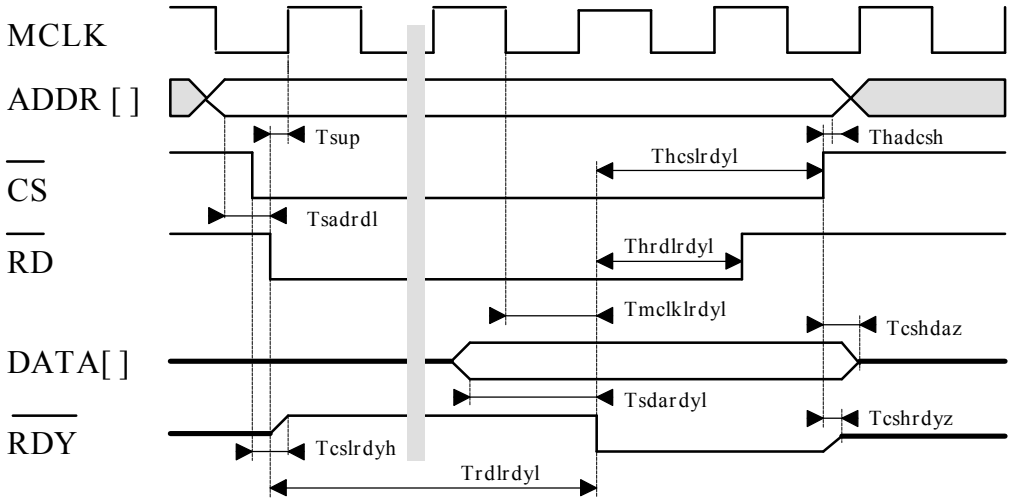
AC Timings

Microprocessor interface (write cycle)



Symbol	Parameter	Min	Typ	Max	Test Conditions
Tfmclk	MCLK frequency	16Mhz	20Mhz		
Tdmclk	Duty cycle of MCLK	40%	50%	60%	
Tsup	Setup (/WR + /CS)low to MCLK rising edge	20 ns			
Tsadwrl	Setup Address to /WR low	0 ns			
Thadcsh	Hold Address to /CS high	0 ns			
Tsdardyl	Setup Data valid to /RDY low	1 MCLK			
Thdardyl	Hold data from /RDY low	0 ns			
Twrlrdyl	Delay from (/WR + /CS) low to /RDY low	3 MCLK		10 MCLK	
Thwrlrdyl	Hold /WR low from /RDY low	20ns			
Thcslrdyl	Hold /CS low from /RDY low	20ns			
Tmclklrdyl	Delay from MCLK falling edge to /RDY low			20 ns	
Tcslrdyh	Delay from /CS low to /RDY high			20 ns	
Tcshrdyz	Delay from /CS high to /RDY Z			30 ns	

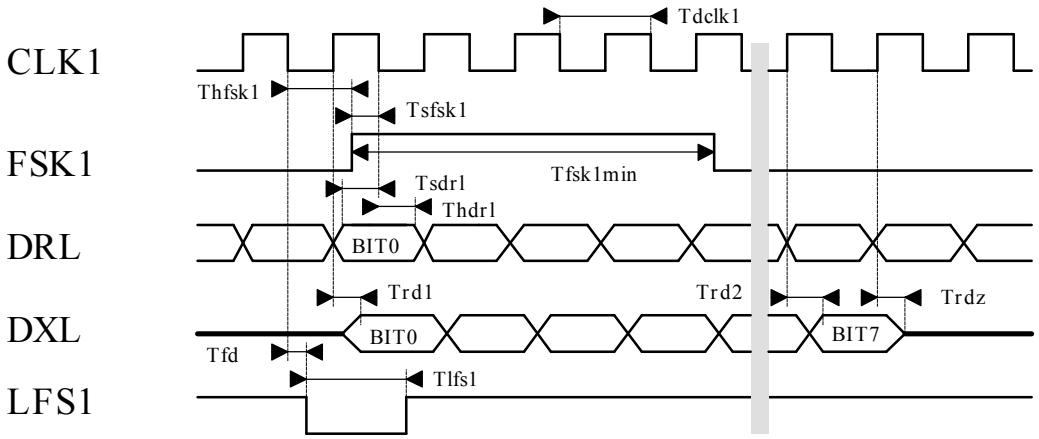
Microprocessor interface (read cycle)



Symbol	Parameter	Min	Typ	Max	Test Conditions
Tsadrdl	Setup Address to /RD low	0 ns			
Thadcsh	Hold Address to /CS high	0 ns			
Tsup	Setup (/RD+ /CS) low to MCLK rising edge	20 ns			
Thrdlrdyl	Hold /RD low from /RDY low	20ns			
Thcslrdyl	Hold /CS low from /RDY low	20ns			
Tsdardyl	Setup data to /RDY low	0.5 MCLK			
Trdlrdyl	Delay from (/RD + /CS) low to /RDY low	3 MCLK		10 MCLK	
Trdhdaz	Delay from /RD high to data Z			30 ns	
Tmclklrdyl	Delay from MCLK falling edge to /RDY low			20 ns	
Tcslrdyh	Delay from /CS low to /RDY high			20 ns	
Tcshrdyz	Delay from /CS high to /RDY Z			40 ns	

Important : /RD, /CS, /WR may be asynchrounous with respect to MCLK, however"tsup" setup time to the following MCLK rising edge must be respected to insure that this rising edge will trig the internal R/W cycle, otherwise an additional MCLK delay will be added to this R/W cycle time.

29C96 interface (Line side - Timing slave)

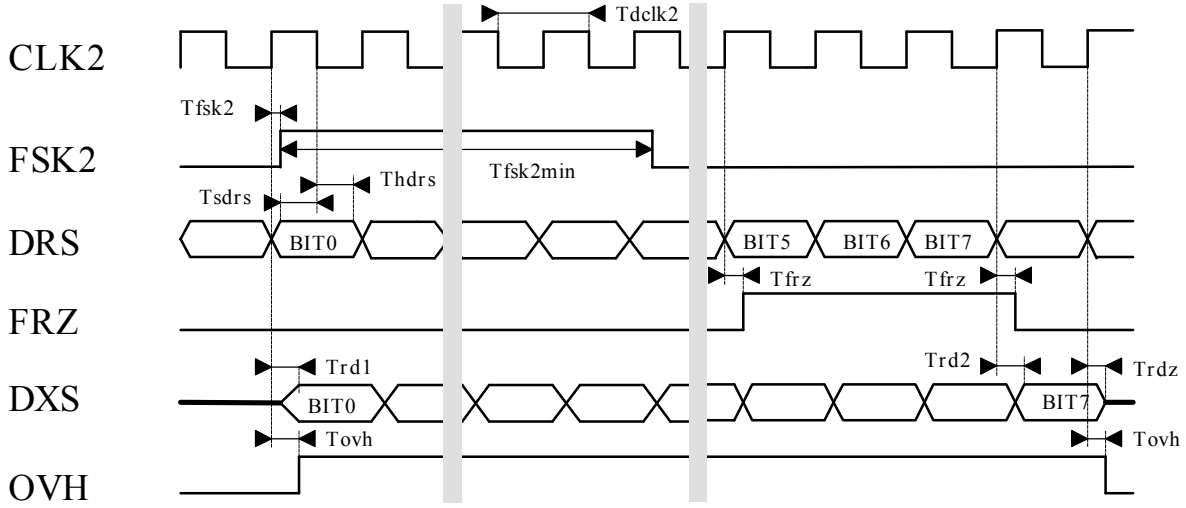


Symbol	Parameter	Min	Typ	Max	Test Conditions
Tdclk1	CLK1 duty cycle	40%	50%	60%	
Tfsk1min	Minimun FSK1 high pulse width	2 CLK1			
Thfsk1(1)	Time between FSK1 rising and CLK1 falling edge	20 ns			
Tsfsk1(1)	Setup FSK1 rising edge before next CLK1 falling edge	20 ns			
Tsdrl	Setup DRL to CLK1 falling edge	20 ns			
Thdrl	Hold DRL from CLK1 falling edge	20 ns			
Trd1	Delay DXL (bit 0) from CLK1 rising edge			40 ns	
Trd2	Delay DXL (bit 7) from CLK2 rising edge			50 ns	
Trdz	Delay DXL Hi Z from CLK1 rising edge			40 ns	
Tfd	Delay LFS1 low from CLK1 falling edge			40 ns	
Tlfs1	LFS1 pulse width		1 CLK1		(2)

NOTE (1) : Thfsk1 and Tsfsk1 describe the available window where FSK1 can be placed to be taken into account to immediatly validate data on DXL and DRL, otherwise, FSK1 will be taken into account on next CLK1 cycle.

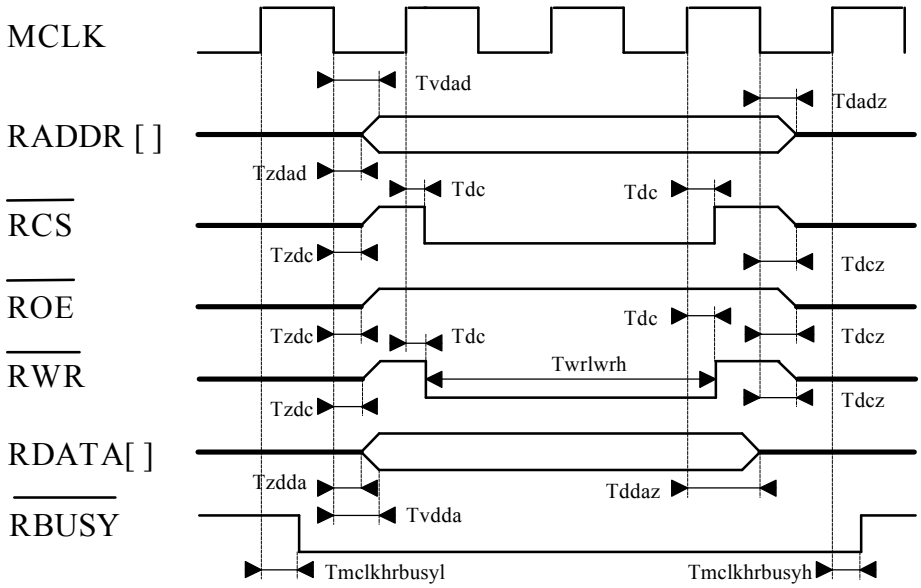
NOTE (2) : LFS1 is generated on the 257th (194th in T1) period of CLK1 from the last FSK1 rising edge.

29C94 interface (System side - Timing Master)



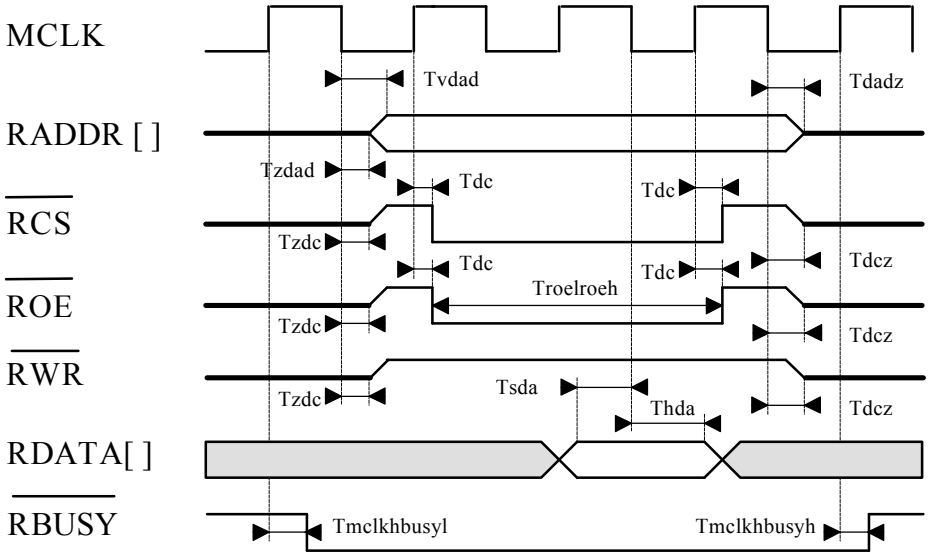
Symbol	Parameter	Min	Typ	Max	Test Conditions
Tdclk2	CLK2 duty cycle	40%	50%	60%	
Tfsk2min	Minimun FSK2 high pulse width		8 CLK2		
Tfsk2	Delay from CLK2 to FSK2 rising edge			50 ns	
Tsdrs	Setup DRS to CLK2 falling edge	20 ns			
Thdrs	Hold DRS from CLK2 falling edge	20 ns			
Trd1	Delay DXS (bit 0) from CLK2 rising edge			40 ns	
Trd2	Delay DXS (bit 7) from CLK2 rising edge			50 ns	
Trdz	Delay DXS Hi Z from CLK2 rising edge			40 ns	
Tfrz	Delay CLK2 rising edge (DRS bit 5 or 7) to FRZ			40 ns	
Tovh	Delay CLK2 rising edge (DXS bit 0 or 7) to OVH			40 ns	

Delay RAM interface (write cycle)



Symbol	Parameter	Min	Typ	Max	Test Conditions
Tmclkhrbusyl	Delay from MCLK to /RBUSY low			30 ns	
Tzdc	Delay from MCLK to command driven			30 ns	
Tdc	Delay from MCLK to command low/high			30 ns	
Tzdad	Delay from MCLK to address driven			35 ns	
Tvdad	Delay from MCLK to address valid			50 ns	
Tzdda	Delay from MCLK to data driven			50 ns	
Tvdda	Delay from MCLK to data valid			55 ns	
Twrlwrh	write pulse width		2 MCLK		
Tdcz	Delay MCLK to command float			50 ns	
Tddaz	Delay MCLK to data bus float			55 ns	
Tdadz	Delay MCLK to address bus float			50 ns	
Tmclkhrbusyh	Delay from MCLK to /RBUSY high			30 ns	

Delay RAM interface (read cycle)



Symbol	Parameter	Min	Typ	Max	Test Conditions
Tmclkhrbusyl	Delay from MCLK to /RBUSY low			30 ns	
Tzdc	Delay from MCLK to command driven			30 ns	
Tdc	Delay from MCLK to command low/high			30 ns	
Tzdad	Delay from MCLK to address driven			35 ns	
Tvdad	Delay from MCLK to address valid			50 ns	
Tsda	Setup data bus to MCLK	20 ns			
Thda	Hold data bus to MCLK	30 ns			
Troelroeh	read pulse width		2 MCLK		
Tdcz	Delay MCLK to command float			50 ns	
Tdadz	Delay MCLK to address bus float			50 ns	
Tmclkhrbusyh	Delay from MCLK to /RBUSY high			30 ns	

Ordering Information